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Enhancement Performance of Co-sputtered Ti-IGZO Thin-Film Transistors with Al-ZrO_2 Gate Dielectric

Cheng-Xiou Lin[1], Shui-Jinn Wang[*1, 2], Rong-Ming Ko[1], Sheng-Yi Wang[1], Hsiang-Yi Chen[1], Chun-Kai Liao[1], Sheng-Tsang Hsiao[1], and Bing-ChengYou[1]

[1]Institute of Microelectronics, Dept. of Electrical Engineering, National Cheng Kung University, Tainan, Taiwan.
[2]Advanced Optoelectronic Technology Center, National Cheng Kung University, Tainan, Taiwan.
*Phone:+886-6-2763882, E-mail:sjwang@mail.ncku.edu

Abstract:

A co-sputtering deposited zirconium aluminum oxide (ZrAlO) gate dielectrics with a dielectric constant ranging from about 27.3 to 15.5 is used for Ti-IGZO thin-film transistors (TFTs). Improved gate controllability and reliability of 50-nm-thick ZrAlO gate dielectrics prepared by a power ratio of ZrO_2:Al_2O_3=100 W:40 W are demonstrated. Using the proposed ZrAlO gate dielectric, it reveals that TFTs with 25-nm-thick Ti-IGZO channel layer exhibit enhanced device performances with subthreshold swing of 110 mV/dec, field effect mobility of 14.89 $cm^2/V{\cdot}s$, on/off current ratio of 1.28×10^7 and positive/negative gate-bias stress of 297 mV/-187 mV, respectively. These performance improvements are attributed to Al incorporation enlarges the energy bandgap of the dielectric and keeps the dielectric layer in amorphous state, and to a considerable reduction in channel defect density after Ti incorporation in IGZO channel.

1. Introduction

In recent years, indium-gallium-zinc oxide (IGZO) thin-film transistor (TFT) devices have drawn much attention due to large driving current and low thermal budget. The highly integrated capability at low temperature is especially required for driving high-resolution organic light-emitting-diode [1]. As one of key building unit of TFTs, gate dielectric plays an important role in switching performance. The influence of the interface between gate dielectric and the semiconductor channel on device performance is a crucial issue. Accordingly, development of suitable gate dielectrics to match well the semiconductor channel is urgently needed [2]. In this study, a matched material structure comprising of ZrAlO layer as the gate dielectric and Ti-IGZO layer as the channel with improved gate controllability and reliability are demonstrated. Effects of Al composition in the ZrAlO dielectrics and Ti in the Ti-IGZO channels on the performance of TFTs through co-sputtering deposition processes are studied. The suitable RF power ratio for the co-sputtering and post-deposition annealing (PDA) temperature for TFT applications are investigated. Positive and negative bias stress tests of the Ti-IGZO TFTs with ZrAlO gate dielectrics are also measured and discussed.

2. Experimental

The schematic structure of Ti-IGZO TFT with a bottom ZrAlO gate dielectrics is shown in Fig. 1. A 50-nm-thick ZrAlO layer was deposited as gate dielectric on n^+-Si wafer by RF co-sputtering of ZrO_2 and Al_2O_3 targets in Ar ambient at room temperature (RT). For the deposition of ZrAlO dielectrics, various sputtering power (0, 30, 40, and 50 W) were used for the Al_2O_3 target with the sputtering power for the ZrO_2 target was kept at 100 W. For comparisons, some samples were subjected to a post-deposition annealing (PDA) at temperature 500 ºC in Oxygen (O_2) ambient for 10 min. Subsequently, a 25-nm-thick Ti-IGZO channel layer was deposited by RF co-sputtering using an IGZO (In_2O_3:Ga_2O_3:ZnO=1:1:1) and TiO_2 targets in Ar ambient at RT with a width-to-length ratio of 200 µm/20 µm. After that, a 25-nm-thick Al-doped ZnO (AZO) as a contact buffer layer deposited by RF sputtering followed by a 150-nm-thick Titanium (Ti) metal electrode deposited by E-beam evaporation were carried out to form source/drain contact pads. Finally, a 200-nm-thick SiO_2 passivation layer was deposited by RF sputtering to prevent devices deterioration.

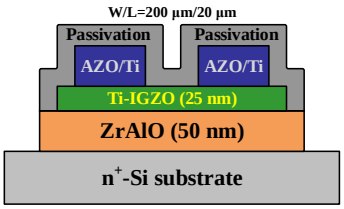


Fig.1 Schematic of the Ti-IGZO TFT with ZrAlO dielectric.

3. Results and Discussion

Through C-V measurement and X-ray photoelectron spectroscopy (XPS) analysis, κ-value and composition contents of ZrAlO dielectrics are summarized in Table I. It shows that κ-value of the ZrAlO dielectric could be adjusted by the co-sputtering power ratio. Four types of α-IGZO TFTs with different dielectric layers, namely device A, B, C, and D, are investigated.

Table I Al ingredients and dielectric constant of ZrAlO films with different co-sputtering power ratios.

Device	Power ratio: ZrO_2(W):Al_2O_3(W)	Al/(Zr+Al) (%)	κ value
A	100:0	0	27.3
B	100:30	11	22.6
C	100:40	15	20.1
D	100:50	20	15.5

Figure 2(a) shows the XRD analysis of ZrO_2 and ZrAlO films without and with PDA for 10 min in O_2 at 500 ºC. It shows that the deposited ZrO_2 layer has a polycrystalline structure regardless of

annealing. In contrast, the co-sputtering ZrAlO layers all have amorphous structure in which a lower leakage current can be expected. Figure 2(b) shows the J-V curve of capacitors with ZrO_2 and ZrAlO films. Note that all dielectric layers have the same EOT of 10 nm. A considerable decrease in leakage current is seen from samples with Al incorporation, which is attributed to Al incorporation enlarges the energy bandgap of the dielectric and keeps the dielectric layer in amorphous state. Our results suggest that device C with Al/(Zr+Al)=15 % has the lowest leakage current among the prepared samples.

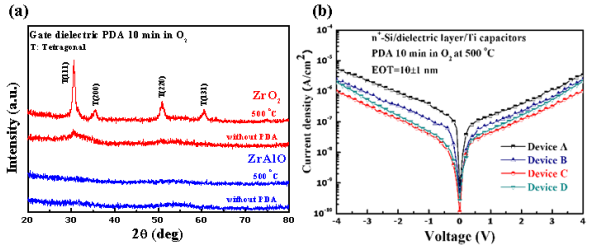
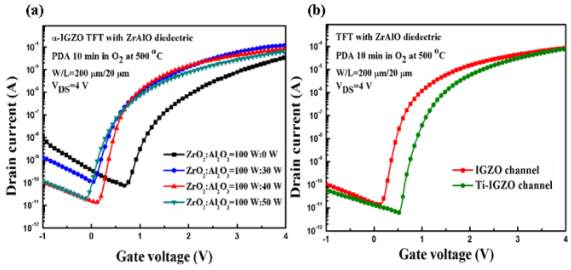


Fig. 2 (a) XRD analysis of ZrO_2 and ZrAlO films without and with PDA for 10 min in O_2 at 500 °C. (b) The J-V curve of n^+-Si/ZrAlO /Ti capacitor structure.

Figure 3(a) shows the transfer characteristics of the α-IGZO TFTs with ZrO_2 and ZrAlO gate dielectrics. It is found that α-IGZO TFT with ZrO_2: Al_2O_3=100 W:40 W (device C) shows the best electrical performance with I_{on}/I_{off} of 6.31×10^6, the lowest subthreshold swing (SS) of 113 mV/dec and highest field-effect mobility (μ_{FE}) of 11.37 $cm^2/V\cdot s$. It suggests that suitable incorporation of Al in ZrO_2 could improve the interface to α-IGZO



and enhance gate controllability.

Fig. 3 Effect of (a) Al incorporation in ZrO_2 gate dielectric and (b) Ti incorporation in IGZO channel on the transfer characteristics of TFTs.

Effect Ti incorporation in α-IGZO channel on TFT performance is also studied. Figure 3(b) shows the comparison of transfer characteristics of TFTs with Ti (called device E) and that of device C (without Ti incorporation). Note that the same fabrication condition was used for the ZrAlO gate dielectric. It reveals that the electrical performance of TFT with Ti incorporation in IGZO has been further improved with I_{on}/I_{off} of 1.28×10^7, subthreshold swing (SS) of 110 mV/dec and field-effect mobility (μ_{FE}) of 14.89 $cm^2/V\cdot s$. Such improvements could be attributed to highly-oxidizable Ti incorporation reduces oxygen vacancy in the IGZO channel and improves the quality of the dielectric/channel interface, as reflected by the further improved SS and μ_{FE}. A comparison of device electrical parameters are also listed in Table II.

Results of gate bias stress (GBS), at positive (+4 V) and negative (-4 V), on the transfer characteristics of device E are shown in Fig. 4. It shows that positive (negative) GBS results in a positive (negative) ΔV_{TH} shift which increases with increasing the stress time (Fig. 5), which could be caused by electron trapping (de-trapping) in dielectric or at dielectric/channel interface. As compared with results of GBS obtained from device C, a considerable decrease in ΔV_{TH} shift suggests the effectiveness of Ti incorporation in improving the quality of dielectric/channel interface and reducing defect density in the channel layer.

Table II Comparisons of device parameters of TFTs.

Device	I_{on}/I_{off}	SS (mV/dec)	V_{TH} (V)	μ_{FE} ($cm^2/V\cdot s$)	D_{it} ($cm^{-2}eV^{-1}$)
A	5.24×10^5	183	1.12	6.74	5.73×10^{12}
B	1.05×10^6	146	0.35	8.93	4.57×10^{12}
C	6.31×10^6	113	0.47	11.37	3.53×10^{12}
D	3.33×10^6	151	0.29	9.15	4.72×10^{12}
E	1.28×10^7	110	0.89	14.89	3.41×10^{12}
[3]	8×10^7	150	0.3	12.5	5.13×10^{11}
[4]	3.7×10^8	131	1.09	-	-

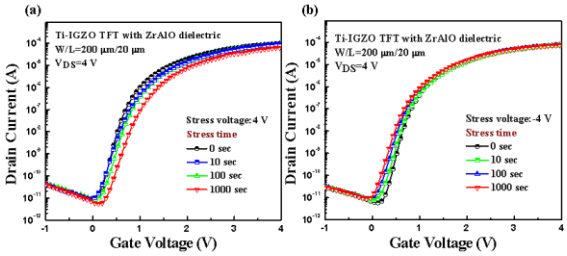


Fig. 4 Ti-IGZO TFT transfer characteristics with ZrAlO gate dielectric (a) PGBS (b) NGBS for different stress times.

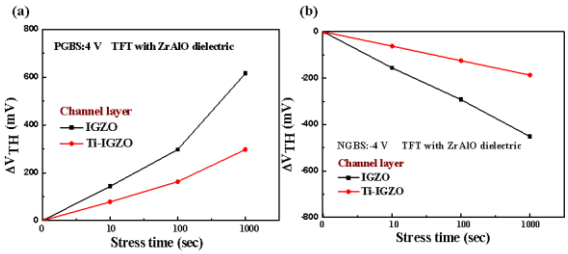


Fig. 5 ΔV_{TH} shift as a function of the stress time of device C and device E.

4. Conclusion

Improved performance of Ti-IGZO TFTs with ZrAlO gate dielectrics have been successfully fabricated by co-sputtering technique. Significantly improved device performance with SS (110 mV/dec), μ_{FE} (14.89 $cm^2/V\cdot s$) and threshold voltage shift from 616 mV to 297 mV in PGBS and from -452 mV to -187 mV in NGBS have been obtained from device E. Our experiments show that Al in corporation in ZrO_2 gate dielectric and Ti incorporation in IGZO channel layer could improve the quality of dielectric/channel interface and reduce defect density in the channel layer, which might be a matched material system for TFT applications.

Acknowledgements

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