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Mechanism of Threshold Voltage Control by Back Gates in CAAC-IGZO FETs

Ryunosuke Honda, Kazuki Tsuda, Toshihiko Takeuchi, Katsuaki Tochibayashi, Tomoaki Atsumi, Kiyoshi Kato and Shunpei Yamazaki

Semiconductor Energy Laboratory Co., Ltd.
398 Hase, Atsugi, Kanagawa, 243-0036, Japan
Phone: +81-46-248-1131, Fax: +81-46-270-3751, E-mail: rh1323@sel.co.jp

Abstract

In *c*-axis aligned crystalline In-Ga-Zn oxide field-effect transistor (CAAC-IGZO FET) fabrication, CAAC-IGZO films are formed on an insulator by the deposition process; thus, multi-gate FETs are fabricated easily. In this study, we fabricated CAAC-IGZO FETs with back gates and investigated their electrical characteristics. With negative V_{BG}, V_{th} shifted to the positive direction with the shape of the V_{FG}-I_D curve maintained. Because CAAC-IGZO FETs have a feature that the subthreshold region extends up to extremely low current, one FET with its back gate achieves suitable characteristics for various applications.

1. Introduction

In recent years, field-effect transistors with *c*-axis aligned crystalline In-Ga-Zn oxide active layers (CAAC-IGZO FETs) have been investigated actively [1, 2]. CAAC-IGZO FETs have an extremely low off-leakage current [3] and high resistance to short-channel effects [4, 5]. Because of such features, CAAC-IGZO FETs have been proposed to be used for large-scale integration [6, 7].

In the fabrication process, CAAC-IGZO films are formed on an insulator by the deposition process. Therefore, the FET structure has high flexibility. The gate can be located either above or below the active layer or both [8], that is to say, it is easy to fabricate a multi-gate structure. The following driving method for multi-gate FETs is suggested: back gates to which voltage different from that of front gates is applied are provided (this structure is referred to as "multiple-independence gate") [9, 10]. It is easy to separately form front and back gates for CAAC-IGZO FETs, and controlling the threshold voltage using the back gate was proposed [11].

This paper describes threshold voltage control using a back gate. We fabricated CAAC-IGZO FETs with back gates and investigated the V_{FG}-I_D characteristics with various V_{BG}. The V_{th} control mechanism is discussed on the basis of a capacitance model. Finally, we propose that V_{th} control using a back gate is a method that capitalizes on the extremely low off-leakage current of CAAC-IGZO FETs.

Although the threshold voltage V_{th} is determined by an $\sqrt{I_D}$ extrapolation method in this report, we confirmed that the contents of discussion also apply to the case where the definition of threshold voltage is different, for example, threshold voltage is determined by a constant current method.

2. Measurement results

First, fabricated CAAC-IGZO FETs are described. Although the FET structure is roughly the same as the trench-gate self-aligned (TGSA) structure that we reported before [12, 13], FETs shown in this report have back gates. Figure 1 shows the cross-sectional transmission electron microscope (TEM) images of an FET with a back gate. The back gate insulators (BGIs) have 30-nm equivalent oxide thickness (EOT) and IGZO films as the active layers have a thickness of 17 nm. The front gate insulators (FGIs) have the following three conditions: 6.1-nm EOT, 8.0-nm EOT, and 11.2-nm EOT. The channel length and the channel width are 0.37 μm and 0.24 μm, respectively.

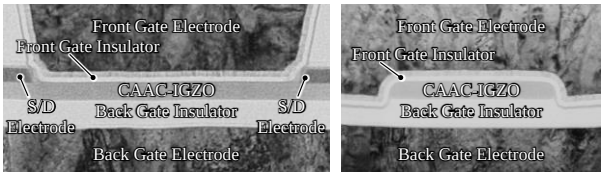

Fig. 1. Cross-sectional TEM image of CAAC-IGZO FET
Left: *L*-direction Right: *W*-direction

Figure 2(a) shows the V_{FG}-I_D curves of an FET with t_{FGI} of 6.1-nm EOT. By applying negative voltage to the back gate, the V_{FG}-I_D curves shifted to the positive direction. The V_{FG}-I_D curves with the *x*-axis indicating $V_{FG}-V_{th}$ are shown in Fig. 2(b). The curves with different V_{BG} almost overlap each other. This suggests that the change by negative voltage application to the back gate is only V_{th}. Figures 2(c) and (d) show V_{FG}-I_D curves of FETs with t_{FGI} of 8.0-nm EOT and 11.8-nm EOT, respectively. The thicker t_{FGI} is, the more noticeably V_{th} is shifted. In Fig. 3, V_{th} is plotted relative to V_{BG}. In the data of each of these FGI thicknesses, V_{th} is the linear function of V_{BG}.

Figure 4 shows gradient of V_{th} in V_{BG} ($\partial V_{th}/\partial V_{BG}$) and subthreshold swing (*S.S.*) as the functions of t_{FGI}. $\partial V_{th}/\partial V_{BG}$ has a linear relationship with t_{FGI}, and the intercept of the approximate straight line is close to 0 V/V. *S.S.* has also a linear relationship with t_{FGI}, and the intercept of the approximate straight line is close to 60 mV/dec.

3. Mechanism of threshold voltage control by back gate

Impurity doping for V_{th} control is not performed in the fabrication process of CAAC-IGZO FETs. With $V_{FG} \leq V_{th}$, the concentration of space charge is low and thus does not affect band bending so much. Therefore, the channel region with $V_{FG} \leq V_{th}$ can be approximated to a simple capacitance model (Fig. 5).

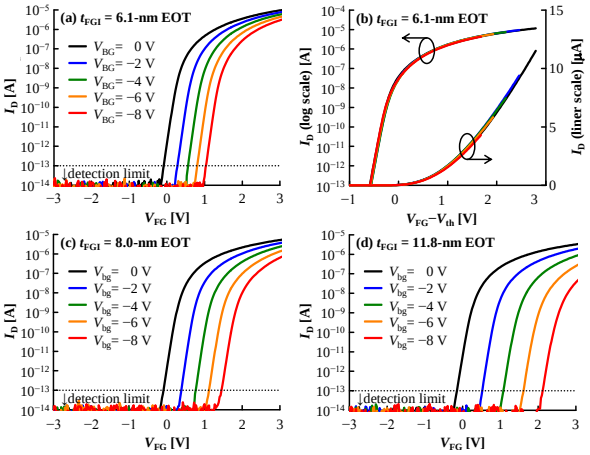

Fig. 2. V_{FG}-I_D curves (V_D=1.2V) (a), (b): t_{FGI} = 6.1-nm EOT (c): t_{FGI} = 8.0-nm EOT (d): t_{FGI} = 11.2-nm EOT

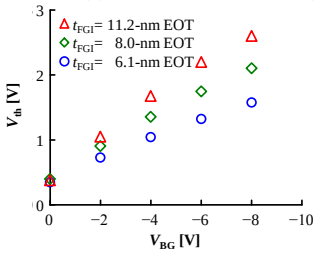

Fig. 3. V_{th} as a function of V_{BG} The average of 8 samples

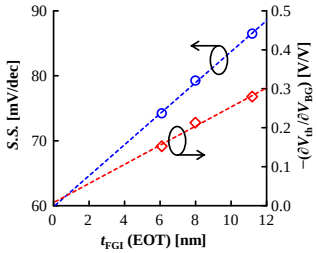

Fig. 4. $\partial V_{th}/\partial V_{BG}$ and *S.S* The average of 8 samples

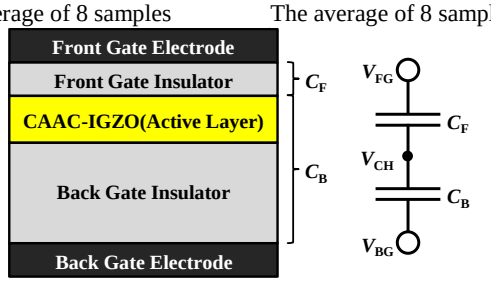

Fig. 5. Capacitance model of channel region of CAAC-IGZO FET

Note that V_{CH} represents the potential at the front channel, that is, the interface between CAAC-IGZO and FGI; C_F, the capacitance above the front channel; and C_B, the capacitance below the front channel. The gradient of V_{CH} in V_{FG} or V_{BG} is represented by the following formulas.

$$\frac{\partial V_{CH}}{\partial V_{FG}}=\frac{C_F}{C_F+C_B},\ \frac{\partial V_{CH}}{\partial V_{BG}}=\frac{C_B}{C_F+C_B} \qquad (1,2)$$

Assuming that V_{CH} with V_{FG}=V_{th} is constant regardless of V_{BG}, the following formula for $\partial V_{th}/\partial V_{BG}$ is established.

$$\frac{\partial V_{th}}{\partial V_{BG}}=-\frac{C_B}{C_F} \qquad (3)$$

This formula suggests that $\partial V_{th}/\partial V_{BG}$ has a straight line with the opposite sign slope of the ratio of C_B to C_F.

Furthermore, on the basis of the same capacitance model, *S.S* is expressed by the following formula.

$$S.S.=\ln(10)\frac{kT}{q}\left(1+\frac{C_B}{C_F}\right)=\ln(10)\frac{kT}{q}\left(1-\frac{\partial V_{th}}{\partial V_{BG}}\right) \qquad (4)$$

As described above, both $\partial V_{th}/\partial V_{BG}$ and *S.S.* depend on the ratio of C_B to C_F. To design the electrical characteristics of CAAC-IGZO FETs with back gates, both C_B and C_F, especially t_{FGI} and t_{BGI}, are important.

4. Off-current control by back gate

As discussed in the introduction, CAAC-IGZO FETs have the feature of an extremely low off-leakage current. Therefore, in the wide range of V_{FG}≤V_{th}, I_D follows the subthreshold characteristics and is the exponential function of V_{FG}. In order to evaluate an extremely low current, we proposed that tens of thousands or more FETs are connected in parallel and that a data retention test circuit is used [14]. Figure 6 shows a V_{FG}-I_D curve obtained using these methods. The subthreshold region extends up to extremely low current. The subthreshold current of CAAC-IGZO FETs significantly decreases when V_{th} is positively shifted by a negative back gate voltage (as shown in Fig. 7).

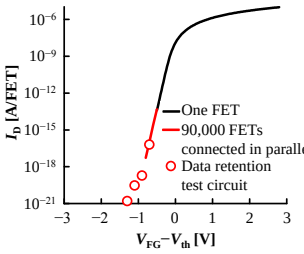

Fig. 6. V_{FG}-I_D curve measured by high precision methods (V_D=1.2V)

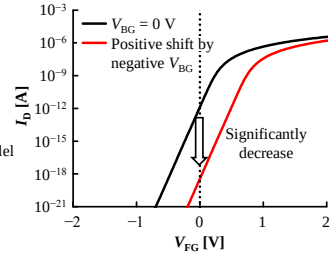

Fig. 7. Subthreshold current decrease by negative V_{BG}

5. Conclusions

We fabricated CAAC-IGZO FETs with back gates and investigated their electrical characteristics. With negative V_{BG}, V_{th} positively shifted with the shape of V_{FG}-I_D curve maintained, and V_{th} is the linear function of V_{BG}. To design the electrical characteristics by V_{th} control using a back gate, both t_{BGI} and t_{FGI} are important.

Since CAAC-IGZO FETs have the subthreshold characteristics in the wide range of V_{FG}≤V_{th}, the subthreshold current is significantly changed by V_{th} control using the back gate. One CAAC-IGZO FET with its back gate achieves suitable characteristics for various applications.

References

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