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The Inverted-Staggered InGaZnO TFT with Hydrogen-Free PECVD-SiO_2 Etch-Stopper and Passivation Layers

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Abstract

It is required to solve the problem of the bottom-gate InGaZnO thin-film transistor (IGZO TFT) equipped with etch-stopper and passivation layers caused by hydrogen contained in the conventional plasma-enhanced chemical vapor deposition (PECVD) process using SiH_4. We proposed and demonstrated the IGZO TFT using hydrogen-free PECVD as a silicon source of tetra-isocyanate-silane ($Si(NCO)_4$). The TFT shows an excellent transfer characteristic without hysteresis.

1. Introduction

Amorphous oxide semiconductor represented by InGaZnO (IGZO) are employed in thin film transistors (TFTs) [1]. Compared with the conventional amorphous Si TFTs, IGZO TFTs have superior device performance, such as high mobility and low off current. However, in order to adopt them in the backplane of an active matrix organic light emitting diode (AMOLED) display, it is necessary to improve the stability of threshold voltage (V_{th}) under both the positive bias stress [2-8] and the negative bias illumination stress [9-14].

As a cause of instability of V_{th}, the influence of hydrogen has been reported in the case of a conventional bottom-gate IGZO TFT with an etch-stopper layer (ESL) and a passivation layer (PL) directly formed on a channel layer (CL) by plasma-enhanced chemical vapor deposition (PECVD) using SiH_4 [7]. Plasma treatment using N_2O toward the CL prior to the capped SiO_2 deposition has also been proposed [5], but it is not sufficient to achieve both in-plane stability and uniformity in mass production.

On the other hand, it has been studied PECVD using raw materials not containing hydrogen. Idris *et al.* have fabricated SiO_2 films by PECVD using tetra-isocyanate-silane ($Si(NCO)_4$, TICS) as a Si source [15,16].

Toward realization of highly stable IGZO TFT and its manufacturing process, we propose a hydrogen-free process. In this paper, we fabricated and characterized bottom-gate IGZO TFTs with the ESL and the PL of SiO_2 deposited by PECVD using TICS and O_2, as compared with the conventional process using SiH_4 and N_2O.

2. Experimental Details

Device Fabrication

An inverted-staggered IGZO TFT with SiO_2 ESL and PL, which channel wide/length were 20/10μm, was fabricated on a non-alkaline glass substrate, as shown in Fig. 1. A SiN_x (50nm) and SiO_2 (300nm) stacked layer was formed by PECVD as a gate insulator (GI) with a temperature of 350℃, over a patterned Mo (200nm) gate electrode. A 50-nm-thick IGZO CL was deposited by dc magnetron sputtering in a mixed gas of Ar and O_2 at 100℃ using a target of In:Ga:Zn = 1:1:1 in atomic ratio and then patterned by photolithography and wet etching. And then IGZO CL was annealed in air at 400℃ for 1hour. The ESL (100nm) and PL (200nm) for "SiH_4-TFT" were used the SiO_2 films which deposited by PECVD using SiH_4 and N_2O at 200℃ (SiH_4-SiO_2 films), and also those for "TICS-TFT" were used the films which deposited using TICS and O_2 at 350℃ (TICS-SiO_2 films). After their ESLs deposition, they were patterned and then Mo (150nm) source/drain electrode (S/D) was formed by combining sputtering and photolithography. Their PLs were deposited and the TFTs were annealed at 300℃ in air for 1hour. Finally, contact holes of both S/D and gate were patterned.

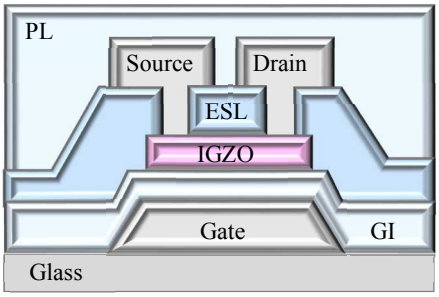

Fig. 1. Schematic cross-sectional view of the inverted-staggered IGZO TFT with ESL and PL.

Characterization

Impurities and I-V curves of SiH_4-SiO_2 and TICS-SiO_2 films were analyzed by secondary ion mass spectrometry (SIMS) and observed by the metal-insulator-semiconductor structure that were composed of both Al dotted electrode and Si substrate, respectively.

The effect of each process against the IGZO CL was directly evaluated by preparing a SiO_2 (100nm) / IGZO (50nm) structure on a glass substrate under the same conditions as forming CL and ESL on device fabrication and measuring the carrier concentration of the IGZO layer by Hall effect using the Van der Pauw method.

Transfer characteristics of the TFTs were measured on a semiconductor parameter analyzer, Agilent 4155C.

3. Results and Discussion

The hydrogen content in a TICS-SiO_2 film, which is prepared with a deposition rate of 170nm/min and a temperature of 350℃ on a Si substrate, has achieved low concentration such as $4x10^{20}$ atoms/cm^3, less than $1x10^{21}$ atoms/cm^3 including in a SiH_4-SiO_2 film with 80nm/min and 200℃. The TICS-SiO_2 film is lower than the hydrogen concentration of the general PECVD film using SiH_4 or tetra-ethoxy-silane.

Figure 2 shows I-V curves of the SiH_4-SiO_2 and TICS-SiO_2 films. Their leakage currents were $4x10^{-11}$ A/cm^2 and $2x10^{-11}$ A/cm^2 at 2 MV/cm, respectively. And their breakdown voltages were 9.1 MV/cm and 11.3 MV/cm at $1x10^{-6}$ A/cm^2, respectively. Although the hydrogen concentration of the TICS-SiO_2 film is low as a low-temperature deposited film, it never leads to defect formation and it shows excellent insulation equal to or higher than the SiH_4-SiO_2 film. On the other hand, the deposition of the TICS-SiO_2 film tends to require higher RF power than that of the SiH_4-SiO_2 film.

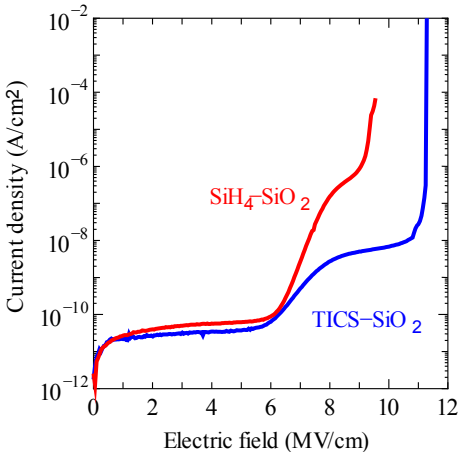

Fig. 2. I-V curves of TICS-SiO_2 and SiH_4-SiO_2 films.

The carrier concentrations of a single IGZO layer, the layer after deposition of the SiH_4-SiO_2 film, and that of the TICS-SiO_2 film were $4x10^{12}$, $1x10^{18}$, and $<1x10^{12}$/cm^3, respectively. Carriers due to defects, *e.g.*, O-vacancy, were generated in the IGZO layer during the SiH_4-SiO_2 process, whereas in the TICS-SiO_2 process carrier generation did not occur and its reduction was observed.

Transfer characteristics of IGZO TFTs, SiH_4-TFT and TICS-TFT, at drain voltage (V_d) of 5V are shown in Fig. 3. In the SiH_4-TFT, the drain current (I_d) cannot be controlled and turned on/off within the range of the gate voltage (V_g) -15V to +20V. Its high conductivity between drain and source is generated by carriers having CL defects caused by a TFT fabrication process using the SiH_4-SiO_2 layer as its ESL. On the other hand, the TFT characteristic of TICS-TFT is clearly shown and has little hysteresis, resulting that the TICS-SiO_2 process involves much less defect generation than the SiH_4-SiO_2 process. The filed-effect mobility, the V_{th}, and the subthreshold swing calculated from its characteristic are 10.3 cm^2/Vs, 5.2 V, and 0.31 V/decade, respectively.

As low temperature and low deposition rate as 200℃ and 80nm/min, respectively, were chosen to suppress the reaction with hydrogen on the SiH_4-SiO_2 process, but as a result the

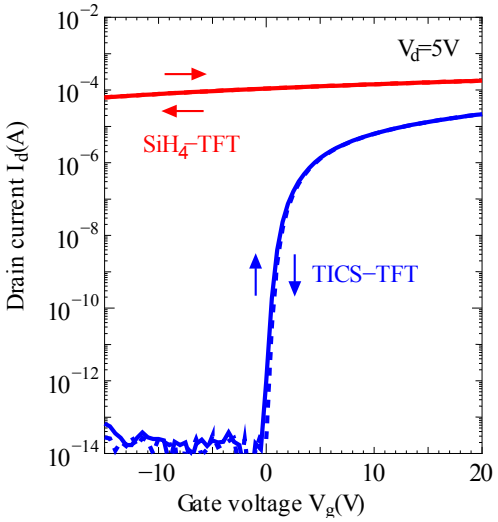

Fig. 3. Transfer characteristics of IGZO TFTs.

effect was not sufficient under the process conditions. This is almost the same as the phenomena which occurred even at 170℃ in the other report[7]. The TICS-SiO_2 process has less influence on the CL despite using both a temperature of 350℃ and a deposition rate of 170nm/min. The processing temperatures including such as GI, CL, ESL, PL, and post deposition annealing are uniform in the range of 300℃ to 400℃, which contributes to the stability of TFT manufacturing process.

4. Conclusion

We have proposed IGZO TFT including PECVD-SiO_2 using raw material not containing hydrogen, TICS, for ESL and PL and evaluated by comparison with PECVD-SiO_2 using conventional SiH_4. We have demonstrated that TFT does not operate within the range of practical V_g using SiH_4-SiO_2, but TFT with TICS-SiO_2 shows good TFT operation without hysteresis.

It is promising as a process for producing highly stable IGZO TFT with suppressing generation of defects by hydrogen.

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