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Analysis and Optimization of Device Parameters on Super-Steep Subthreshold Slope PN-Body Tied SOI-FET

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Abstract

Characteristics of the super-steep subthreshold slope (SS) "PN-body tied (PNBT) silicon-on-insulator field-effect transistor (SOI-FET)" dependence on each of the device parameters were investigated by using TCAD simulation. The SS characteristics are improved by N-region width scaling and optimization of impurity concentration in the N-region. Additionally, for the first time, it is clarified that the PNBT SOI-FET needs to be partial depletion to occur the super-steep SS.

1. Introduction

Recently, steep subthreshold slope (SS) devices (<60mV/dec), such as tunnel field-effect transistors (FETs) and negative capacitance FETs have been studied for ultralow power applications. We have proposed the PN-body tied (PNBT) silicon-on-insulator field-effect transistor (SOI-FET) [1], [2], which has achieved super-steep SS (< 1mV/dec) at low drain voltage (V_d = 0.1 V). However, the analysis and optimization of the device parameters are insufficient.

In this study, we investigate the characteristics of the PNBT SOI-FET dependence on each of the parameters by using TCAD simulation. We found out that the SS characteristics are improved by N-region width (W_b) scaling and optimization of impurity concentration in the N-region (N_b). Additionally, it is a key point in the PNBT SOI-FET whether the condition under the channel is partial depletion.

2. Simulation Conditions and Results

2.1 Device Structure and Operation Mechanism

Fig. 1 shows the device structure of the N-channel PNBT SOI-FET. 3D device simulations were done with the structure as shown in Fig. 1 (a) by using HyENEXSS [3]. The PN body region makes up the PNP bipolar junction transistor (BJT) structure, which has a role of the hole injection into the channel region [1]. We consider that the super-steep SS is induced by floating body effects (FBEs) due to the accumulated hole by the hole injection.

2.2 Simulation Model Parameters Fitting

First, we modified simulation model parameters in order to fit the measurement result. Shockley–Read–Hall (SRH) model affects the carrier injection efficiency from the body to the channel region and the carrier accumulation in the channel region. Therefore, it is important parameter on this device. Additionally, the carrier lifetime depends on the fabrication process. Therefore, it needs fitting based on the measured value.

In this section, we used "Actual Measurement Condition" parameters in Table I for comparison of the measurement result with the simulation results. Fig. 2 shows the I_d–V_g characteristics (at the body voltage V_b = 0.8 V) dependence on the carrier lifetime of SRH model and also shows the measured result [4]. When the carrier lifetime is shortened, the trigger voltage to occur super-steep SS shifts to positive direction, which approximates the measurement result. Therefore, we set carrier lifetime "×0.01" in the following simulation.

2.3 Analysis and Optimization of Device Parameters

We varied one of the device parameters for the analysis and optimization while the other parameters fixed. In this section, "Simulation Standard Condition" parameters in Table I were used as the standard parameters. Fig. 3 shows the I_d–V_g characteristics dependence on W_b. When W_b is narrowed, the trigger voltage to occur super-steep SS shifts to negative direction and the I_{ON}/I_{OFF} ratio improves. Narrowing W_b is equivalent to shortening base length of the PNP-BJT. Therefore, the short W_b improves the SS characteristic of the PNBT SOI-FET. Fig. 4 shows the I_d–V_g characteristics dependence on N_b. When N_b is lowered, the SS characteristic improves. Reduction of N_b also improves the carrier injection efficiency from the body to the channel region. However, the leakage current becomes large at $N_b = 1\times10^{16}$ cm^{-3}. The cause for the leakage current seems to be punch through. N_b should be lowered within the limits of the punch through in order to improve I_{ON}/I_{OFF} ratio while maintaining the super-steep SS.

Fig. 5 shows the I_d–V_g characteristics dependence on the SOI thickness T_{Si}. When T_{Si} is less than 20 nm, the super-steep SS disappears. Fig. 6 shows the hole concentration in the SOI region before on state. Holes accumulate in the SOI region at T_{Si} = 50 nm. In contrast, holes do not accumulate in the SOI region at T_{Si} = 20 nm. Holes discharge from the SOI region to the source due to source-body barrier lowering of the full depletion effect. It is considered that the PNBT SOI-FET uses FBEs, thus the SOI region needs to be partial depletion to accumulate carriers. The maximum depletion width W_{dm} is obtained by following equation (1) [5]:

$$W_{dm} = \sqrt{\frac{4\varepsilon_{si}kT\ln(N_{ch}/n_i)}{q^2N_{ch}}} \quad (1)$$

where ε_{si} is the silicon permittivity, k is the Boltzmann's constant, T is the absolute temperature, N_{ch} is the channel impurity concentration, n_i is the intrinsic carrier density, and q is the elementary charge. In this case ($N_{ch} = 1\times10^{18}$ cm^{-3}), W_{dm} is 32.8 nm. Therefore, the SS characteristic deteriorates when T_{Si} is thinner than W_{dm} as shown in Fig. 5. Fig. 7 shows the

I_d–V_g characteristics dependence on N_{ch}. N_{ch} is the important parameter for the threshold voltage (V_{th}) control; however, when N_{ch} is lowered, the super-steep SS characteristic disappears. The reason for that also comes from diminishing neutral region in the SOI region. The PNBT SOI-FET needs to be partial depletion, which should be considered when designing the device.

3. Conclusions

We simulated and analyzed the PNBT SOI-FET dependence on each of the device parameters, based on the fitted SRH model. The SS characteristics have been improved by W_b scaling and N_b optimization. Additionally, for the first time, we have clarified that the PNBT SOI-FET needs to be partial depletion to occur the super-steep SS. T_{Si} and N_{ch} should be considered when designing the device, especially on the V_{th} control.

Acknowledgements

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References

[1] J. Ida *et al.*, *IEDM Tech. Dig.* (2015) 624. [2] T. Yoshida *et al.*, *Proc. of IEEE S3S Conf.* (2016) 6a.4-1. [3] HyENEXSS^{TM} ver5.5, Selete (2011). [4] T. Mori *et al.*, *JSAP* (2018) 18p-A202-10 [in Japanese]. [5] Y. Taur *et al.*, *Fundamentals of Modern VLSI Devices* (2009) 82.

Table I Simulation conditions.

Device Parameter	Actual Measurement Condition	Simulation Standard Condition
Gate Oxide T_{ox}	4.4 nm	5 nm
SOI Thickness T_{Si}	50 nm	50 nm
Buried Oxide Thickness T_{BOX}	200 nm	200 nm
Gate Length L_g	200 nm	200 nm
Gate Width W_g	1 μm	1 μm
N-region Width W_b	1 μm	1 μm
Channel Impurity Concentration N_{ch}	Obtained by Process Simulation	1×10^{18} cm^{-3}
N-region Impurity Concentration N_b		1×10^{18} cm^{-3}

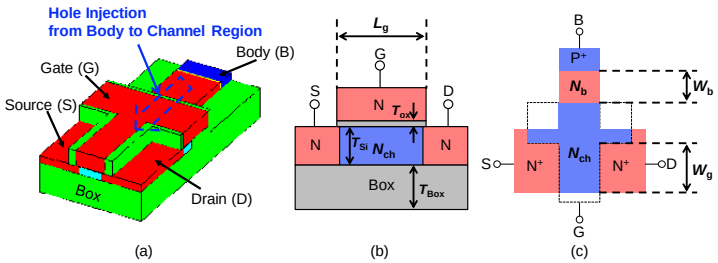

Fig. 1. Device structure of the PNBT SOI-FET. (a) Top-down view. (b) Front view. (c) Plane view.

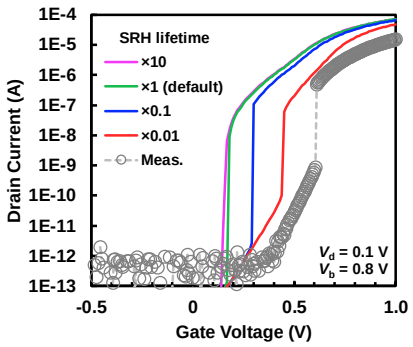

Fig. 2 I_d–V_g characteristics dependence on carrier lifetime of SRH model.

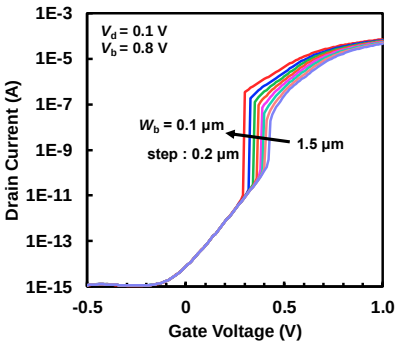

Fig. 3 I_d–V_g characteristics dependence on W_b.

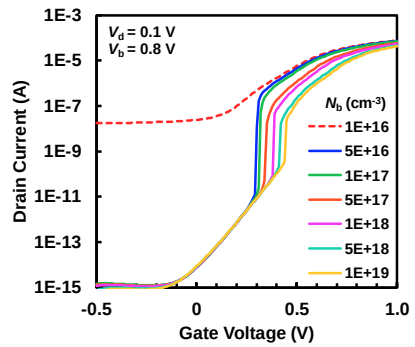

Fig. 4 I_d–V_g characteristics dependence on N_b.

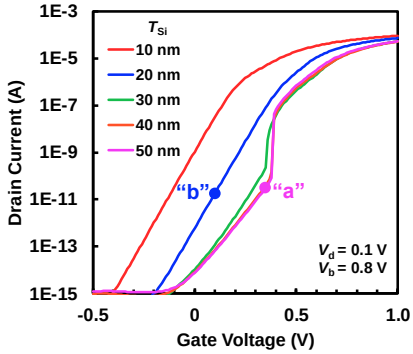

Fig. 5 I_d–V_g characteristics dependence on T_{Si}.

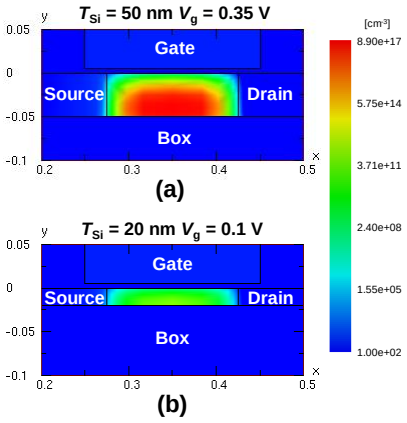

Fig. 6 Hole concentration in SOI region (forefront) before on state. (a) "a" point in Fig. 5. (b) "b" point in Fig. 5.

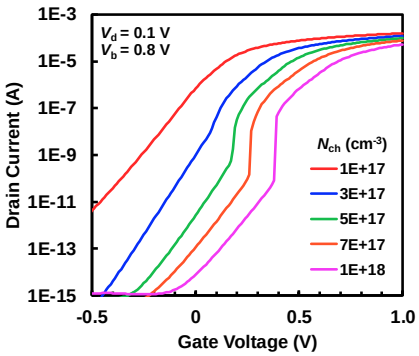

Fig. 7 I_d–V_g characteristics dependence on N_{ch}.