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Performance Analysis of Gate-All-Around Negative Capacitance Stacked Nanowire and Negative Capacitance Nanosheet FETs

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Abstract

In this work, the gate-all-around (GAA) stacked negative capacitance nanowire (NC-NW) and nanosheet (NC-NS) FETs are analyzed comprehensively for the first time. Compared with the 3-stacked (3S) NC-NW FET, 1-stacked (1S) NC-NW FET shows larger maximum internal voltage gain ($A_{v,max}$) due to better capacitance matching, lower minimum subthreshold swing (SS), and larger I_{on} improvements over nanowire (NW) FET. As the vertically stacked number of NW FETs increases, the effective I_{on} per unit width decreases due to the increased series resistance. At low gate bias ($V_{g,ext} \approx 0V \sim 0.16V$), 1S NC-NW FET with larger MOS capacitance (C_{MOS}) operated with positive ferroelectric capacitance ($C_{FE} > 0$) shows lower A_v (at low $V_{g,ext}$) than the 1S NC-NS FET. As gate bias increases, 1S NC-NW FET enters the negative ferroelectric capacitance region ($C_{FE} < 0$), and therefore 1S NC-NW FET exhibits higher $A_{v,max}$ than the 1S NC-NS FET due to its larger C_{MOS}. Besides, 1S NC-NW FET exhibits +90% I_{on} improvements over NW FET, and 1S NC-NS FET shows +44% I_{on} improvements over nanosheet (NS) FET. NW FET exhibits lower DIBL than NS FET due to better electrostatic control, while NC-NW FET shows more significant negative DIBL than the NC-NS FET due to its larger A_v difference between high and low drain bias. NS FET shows larger I_{on} than the NW FET due to higher mobility, and negative capacitance effect reduce the I_{on} difference between NC-NS and NC-NW because NC-NW exhibits larger $A_{v,max}$.

Introduction

For the sub-5nm technology node, the gate-all-around (GAA) FET is a promising candidate owing to its excellent electrostatics and short channel control [1]. GAA nanowire (NW) FETs with better gate control and GAA nanosheet (NS) FETs with large effective width (W_{eff}) are analyzed for performance enhancement [2-3]. Negative capacitance FET (NCFET) [4-6] incorporating a ferroelectric layer in the gate dielectric stack can improve the subthreshold swing (SS) and I_{on}/I_{off} ratio [7-8]. In this work, for the first time, we analyze the SS, internal voltage gain (A_v), I_{on} and negative drain-induced barrier lower (DIBL) of stacked negative capacitance NW (NC-NW) and negative capacitance NS (NC-NS) FETs considering the impact of vertically stacked number of layers.

Device Design and Simulation Methodology

In this work, NW and NS FETs are designed with L_g = 20.2 nm, footprint = 32 nm, diameter = 7 nm, metal thickness (T_m) = 7nm, and EOT = 0.6nm. The mobility of NW and NS FETs are calibrated with the data in [9], and NW FET shows lower mobility than the NS FET due to additional quantum confinement effects. Fig. 1 shows the schematics of 1-stacked (1S) to 3-stacked (3S) NW and NS FETs. For analyzing the NC-NW and NC-NS FETs, the extracted coercive electric field E_c = 1 MV/cm, remnant polarization P_0 = 10 $\mu C/cm^2$ [8], and ferroelectric layer thickness (T_{FE}) = 3 nm are used for hysteresis-free design. The simulation framework [8] of 3D TCAD considering 1S to 3S NW and NS FETs coupled with 1-D Landau-Khalatnikov (LK) ferroelectric equation are used to analyze the NC-NW and NC-NS FETs.

Results and Discussion

Fig. 2(a) shows the charge density(Q_g) comparisons of 1S and 3S NC-NW FETs in the ferroelectric and channel plotted versus V_{FE} (voltage across the ferroelectric layer) and internal gate voltage ($V_{g,int}$) as external gate voltage ($V_{g,ext}$) ranges from 0V ~ 1V. The slope of Q_g vs. V_{FE} indicates the ferroelectric capacitance C_{FE}. For a given change in the internal gate voltage ($\Delta V_{g,int}$), the change in charge density (ΔQ_g) of 1S NC-NW FET is larger than that of 3S NC-NW FET (Fig. 2(a)), and therefore 1S NC-NW FET shows larger C_{MOS} than 3S NC-NW FET as shown in Fig. 3. C_{MOS} is defined as the capacitance underneath the ferroelectric layer as shown in Fig. 2(b). As the vertically stacked number of FET increases, the series resistance increases which decreases ($\Delta Q_g/\Delta V_{g,int}$) and C_{MOS}. At low $V_{g,ext}$ ($\approx$ 0V ~ 0.16V), 1S NC-NW FET is operated with positive C_{FE} (Fig. 2(a)) and therefore exhibits lower internal voltage gain (A_v) at low $V_{g,ext}$ than 3S NC-NW FET (Fig. 4). The definition of internal voltage gain is $A_v \equiv \partial V_{g,int}/\partial V_{g,ext} = |C_{FE}|/(|C_{FE}| - C_{MOS})$. As $V_{g,ext}$ increases, the 1S NC-NW FET enters the negative C_{FE} region, and shows better capacitance matching and larger maximum A_v ($A_{v,max}$) than the 3S NC-NW FET. Therefore, 1S NC-NW shows lower minimum SS than the 3S NC-NW as shown in Fig. 5.

Fig. 6 shows the charge density comparisons of 1S NC-NW and 1S NC-NS FETs. As can be seen, as $V_{g,ext}$ ranges from 0V ~ 1V, 1S NC-NS FET is entirely operated with negative C_{FE}. Therefore, compared with 1S NC-NW FET, 1S NC-NS FET shows better capacitance matching (Fig. 7) and larger A_v (Fig. 8) at low $V_{g,ext}$. 1S NC-NW FET exhibits larger $\Delta Q_g/\Delta V_{g,int}$ (Fig. 6) and larger C_{MOS} (Fig. 7) than the 1S NC-NS FET due to its better electrostatic control. Therefore, as $V_{g,ext}$ increases, the 1S NC-NW FET enters the negative C_{FE} region and shows larger $A_{v,max}$ than the 1S NC-NS FET (Fig. 8). Fig. 9 shows that 1S NC-NW shows lower minimum SS (= 45mV/dec) than the 1S NC-NS FET (= 53mV/dec).

Fig. 10 shows the I_{on}-I_{off} comparisons among NW, NS, NC-NW, NC-NS FETs. As the stacked number of layers increases, I_{on} (per unit width) decreases due to the increased series resistance. NS FETs show larger I_{on} (+64.8%) than NW FETs due to its higher mobility [9]. 1S NC-NW FET shows larger I_{on} improvements (+90% over 1S NW FET) than 3S NC-NW FET (+60% over 3S NW FET) and 1S NC-NS FET (+44% improvements over 1S NS FET) because 1S NC-NW FET exhibits larger $A_{v,max}$. Therefore, 1S NC-NW and 1S NC-NS FETs only exhibit 24.8% difference in I_{on} which is smaller than the I_{on} difference (64.8%) between 1S NS and NW FETs. Fig. 12 shows that NW FET exhibits smaller DIBL than NS FET due to its better electrostatic control, while NC-NW FET exhibits more significant negative DIBL than the NC-NS FET. This is because NC-NW FET shows larger A_v difference (at threshold voltage) between high and low drain bias (Fig. 13) which enlarges the negative DIBL.

Acknowledgements

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References

[1] S. Bangsaruntip et al., *IEDM*, 2009. [2] Y. Seo et al., *SSE*, 2018. [3] N. Loubet et al., *VLSI*, 2017. [4] S. Salahuddin et al., *Nano Lett,* 2008. [5] C. Hu et al., *DRC,* 2015. [6] C.-J. Su et al., *IEDM,* 2017. [7] V. Hu et al., *IEDM,* 2017. [8] P.-C. Chiu et al., *EDTM,* 2018. [9] S. Barraud et al., *IEDM,* 2017.

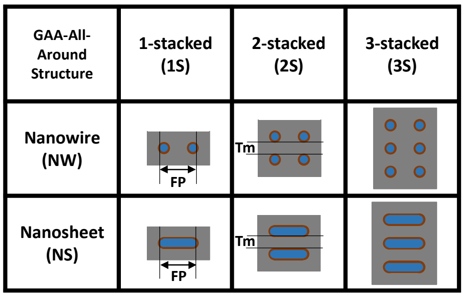

Fig. 1. Schematics of gate-all-around (GAA) stacked nanowire (NW) and nanosheet (NS) FETs. NW and NS FETs are designed with Lg = 20.2 nm, footprint (FP) = 32 nm, diameter = 7 nm, metal thickness (T_m) = 7nm, and EOT = 0.6nm.

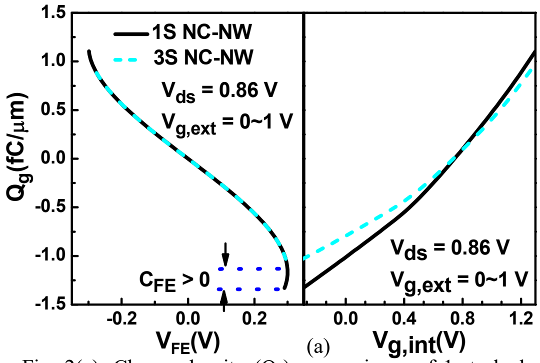

Fig. 2(a). Charge density (Q_g) comparisons of 1-stacked and 3-stacked NC-NW in the ferroelectric and channel are plotted versus V_{FE} (voltage across the ferroelectric layer) and internal gate voltage ($V_{g,int}$) as external gate voltage ($V_{g,ext}$) ranges from 0 ~ 1V.

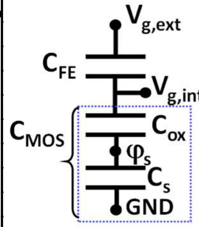

Fig. 2(b). Capacitance model of NCFET. At given Q_g, $V_{g,ext} = V_{FE} + V_{g,int}$.

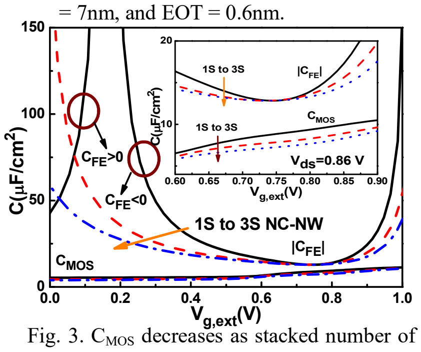

Fig. 3. C_{MOS} decreases as stacked number of NW increases. As stacked number increases, series resistance (Rsd) increases which decreases the induced gate charge (ΔQ_g) at given $\Delta V_{g,int}$, and therefore decreases C_{MOS}.

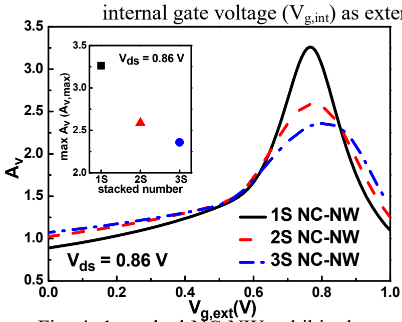

Fig. 4. 1-stacked NC-NW exhibits largest max A_v ($A_{v,max}$) than the 2-stacked and 3-stacked NC-NW due to better capacitance matching ($V_{g,ext}$ = 0.6 ~ 0.88V).

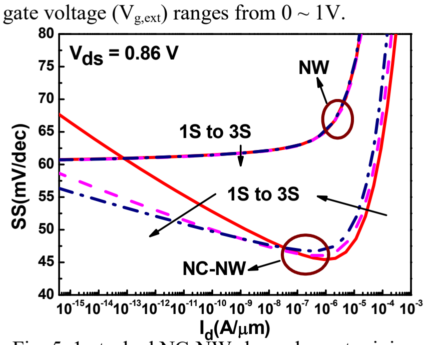

Fig. 5. 1-stacked NC-NW shows lowest minimum subthreshold swing compared with the 2-stacked and 3-stacked NC-NW due to its largest $A_{v,max}$.

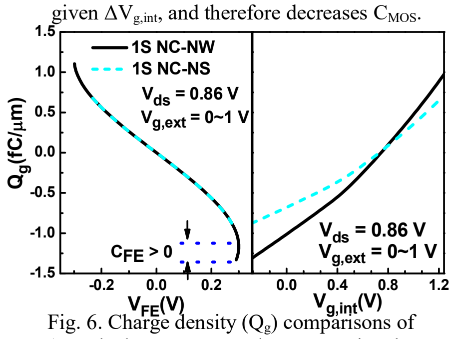

Fig. 6. Charge density (Q_g) comparisons of 1-stacked NC-NW and NC-NS in the ferroelectric and channel are plotted versus V_{FE} and $V_{g,int}$ as $V_{g,ext}$ ranges from 0 ~ 1V.

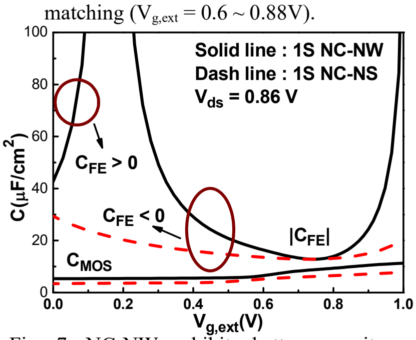

Fig. 7. NC-NW exhibits better capacitance matching at $V_{g,ext} \approx$ 0.6V~0.88V, while NC-NS exhibits better capacitance matching at $V_{g,ext} \approx$ 0V~0.4V. NW exhibits larger C_{MOS} than NS.

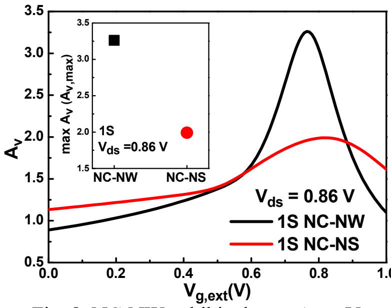

Fig. 8. NC-NW exhibits larger A_v at $V_{g,ext} \approx$ 0.6V~0.88V, while NC-NS exhibits higher A_v at $V_{g,ext} \approx$ 0V~0.4V.

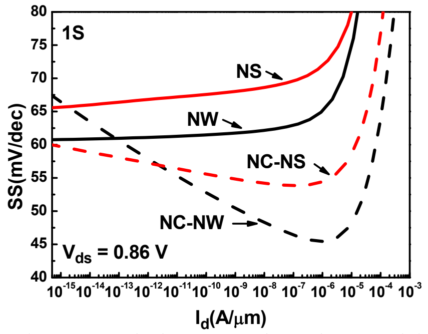

Fig. 9. 1-stacked NC-NW shows lowest minimum subthreshold swing compared with the 1-stacked NC-NW due to its higher $A_{v,max}$ as shown in Fig. 8.

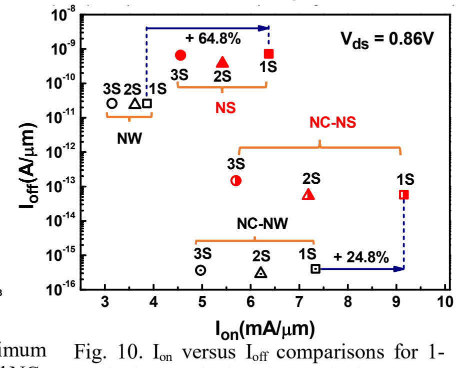

Fig. 10. I_{on} versus I_{off} comparisons for 1-stacked, 2-stacked, and 3-stacked NW, NS, NC-NW, and NC-NS FETs at V_{ds} = 0.86V.

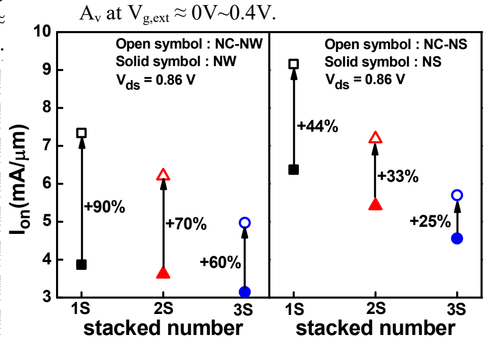

Fig. 11. 1-stacked NC-NW (NC-NS) shows largest I_{on} improvements compared with 2-stacked and 3-stacked NC-NW (NC-NS). NC-NW shows larger I_{on} improvements than NC-NS due to larger $A_{v,max}$. I_{on} improvements = the I_{on} ratio of NC-NW to NW or NC-NS to NS.

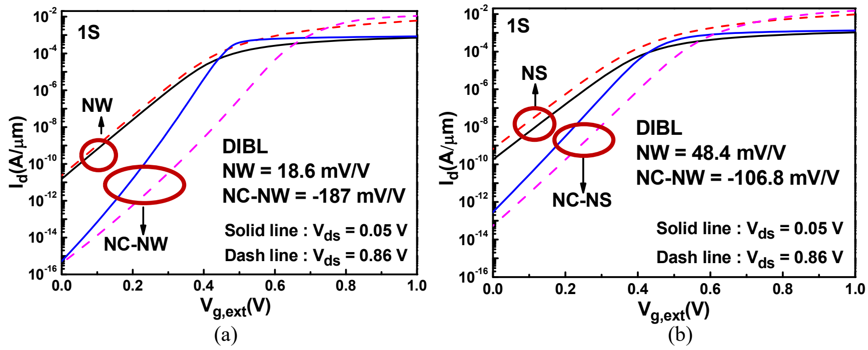

Fig. 12. The I_d-$V_{g,ext}$ characteristics of (a) NC-NW and NW FETs, and (b) NC-NS and NS FETs at V_{ds} = 0.05 V and V_{ds} = 0.86 V, respectively. NC-NW and NC-NS FETs show better subthreshold swing and negative drain-induced barrier lowering (DIBL) compared with the NW and NS FETs.

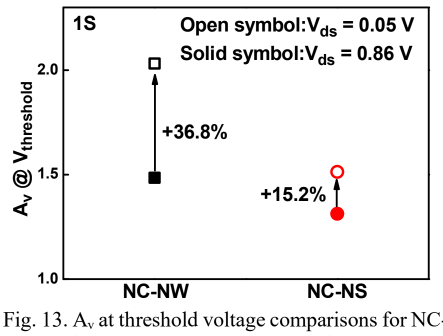

Fig. 13. A_v at threshold voltage comparisons for NC-NW and NC-NS at V_{ds} = 0.05 V and 0.86 V. NC-NW with larger A_v difference between high and low V_{ds} results in larger negative DIBL than NC-NS.