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Stability Analysis of Subthreshold/Superthreshold Negative Capacitance FinFET SRAM Cell

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Abstract

In this work, we analyze the read, write, and hold static noise margins (RSNM, WSNM, and HSNM) for 6T negative capacitance FinFET (NC-FinFET) SRAM cell in the subthreshold and superthreshold regions. In the subthreshold region (V_{DD} = 0.4V), NC-FinFET SRAM cell shows better RSNM (= 84mV) than FinFET SRAM because pass-gate (PG) NC-FinFET operated in the subthreshold and saturation regions exhibits negative differential resistance (NDR) effect and becomes weaker, which reduces the read disturb voltage of NC-FinFET SRAM. Besides, NC-FinFET SRAM shows higher HSNM (= 177mV) than FinFET SRAM due to its lower subthreshold swing induced by negative capacitance effect. At V_{DD} = 0.4V, NC-FinFET SRAM cell shows larger WSNM (= 191mV) than FinFET SRAM cell. This is because PG NC-FinFET with negative capacitance effect becomes stronger in the linear region, and pull-up NC-FinFET with NDR effect becomes weaker in the saturation region. In other words, NC-FinFET SRAM cell resolves the conflict between read and write, and improves RSNM, HSNM and WSNM simultaneously for sub-/near-threshold operation. In the superthreshold region (V_{DD} = 1V), NC-FinFET SRAM cell exhibits 1.73 times larger RSNM (= 183mV) than FinFET SRAM cell, and exhibits adequate WSNM (= 198mV). 6T NC-FinFET SRAM cell performs superior stability in the subthreshold/superthreshold regions.

Introduction

Negative capacitance FET (NCFET) with a ferroelectric layer in the gate dielectric stack shows improved subthreshold swing and Ion/Ioff ratio. NCFET therefore, has emerged as a promising candidate for ultra-low power and high-performance applications [1-4]. Circuit performance analysis of negative capacitance FinFET (NC-FinFET) has been presented [5], and the energy of NC-FinFET can be reduced by ~10x. NC-FinFET SRAM cell has been analyzed at V_{DD} = 0.7V [6]. However, the stability analysis of NC-FinFET SRAM cell operated in the near-/subthreshold region has rarely been examined. In this paper, we analyze the impact of V_{DD} scaling and ferroelectric layer thickness (T_{fe}) on the stability of 6T NC-FinFET SRAM cell compared with FinFET SRAM cell comprehensively. Our results show that for NC-FinFET SRAM cells operated in the subthreshold region, both read and write stability can be improved as T_{fe} increases.

Simulation Framework of NC-FinFET SRAM Cell

In this work, the baseline FinFET is designed with L_g = 20nm, fin width = 8nm, and fin height = 42nm. We use TCAD to analyze the current-voltage, charge-voltage, and capacitance characteristics of the baseline FinFET. We establish the simulation framework for circuit analysis by using lookup table based Verilog-A model including Landau-Khalatnikov equation [7], and then using HSPICE to perform the SRAM simulations. The extracted coercive electric field E_c = 1MV/cm and remnant polarization P_0 = 10μc/cm^2 [3] are used for analyzing NC-FinFET SRAM cells.

Results and Discussion

Fig. 1 shows the I_D-V_G characteristics for NC-FinFETs (T_{fe} = 7nm) and FinFETs (T_{fe} = 0nm) at V_D = 1 V. NC-FinFETs exhibit higher I_{on}/I_{off} ratio, better subthreshold swing (SS), and larger threshold voltage (Vt) than the FinFETs. Fig. 2 shows that as ferroelectric layer thickness (T_{fe}) increases, the read static noise margin (RSNM) increases at V_{DD} ranges from 0.4V to 1V. In the subthreshold region (V_{DD} = 0.4V), NC-FinFET SRAM cell with T_{fe} = 7nm shows 1.44x larger RSNM than the FinFET SRAM cell due to its smaller read disturb voltage ($V_{read,0}$) as shown in Fig. 4. At V_{DD} = 0.4V, pass-gate (PG) NC-FinFET operated in the subthreshold ($V_{GS,PG}$ = 0.4V – $V_{read,0}$) and saturation ($V_{DS,PG}$ = 0.4V – $V_{read,0}$, $V_{read,0}$ = 0.026V) regions shows negative differential resistance (NDR) [8-10] which makes PG NC-FinFET weaker and reduces $V_{read,0}$. RSNM increases as $V_{read,0}$ decreases. In the superthreshold region (V_{DD} = 1V), NC-FinFET SRAM cell exhibits 1.73x larger RSNM than the FinFET SRAM cell due to its larger Vt and better SS. Fig. 3 shows the butterfly curves of RSNM for NC-FinFET and FinFET SRAM cells. Negligible hysteresis window of RSNM is observed for NC-FinFET SRAM cell with T_{fe} = 7nm.

Fig. 5 shows that in the near-/sub-threshold regions (V_{DD} = 0.4V ~ 0.6V), NC-FinFET SRAM cell exhibits larger write static noise margin (WSNM) than the FinFET SRAM cell due to its lower $V_{write,0}$ as shown in Fig. 6. WSNM increases as $V_{write,0}$ decreases. At V_{DD} = 0.4V ~ 0.6V, $V_{write,0}$ decreases as T_{fe} increases. For NC-FinFET SRAM (T_{fe} = 7nm) operated in the subthreshold region (V_{DD} = 0.4V), PG NC-FinFET with negative capacitance becomes stronger in the linear region ($V_{GS,PG}$ = 0.4V, $V_{DS,PG}$ = $V_{write,0}$ = 0.017V), and pull-up (PU) NC-FinFET with NDR becomes weaker in the saturation region ($V_{GS,PU}$ = -0.4V, $V_{DS,PU}$ = $V_{write,0}$ – 0.4V = -0.383V) as shown in Fig. 7(a) and 7(b), which makes NC-FinFET SRAM cell easier to write at sub-/near-threshold regions compared with FinFET SRAM cell. However, in the superthreshold region (V_{DD} = 1V), NC-FinFETs exhibit larger drain saturation voltage [V_{Dsat} = (V_{GS} – V_t)/m], which makes PG and PU NC-FinFETs operated in the linear region during write operation as shown in Fig. 8(b). Therefore, at V_{DD} = 1V, NC-FinFET SRAM cell exhibits lower WSNM than the FinFET SRAM cell. However, NC-FinFET SRAM cell still shows adequate WSNM (= 198mV), which is still larger than RSNM (= 183mV) at V_{DD} = 1V. Fig. 9 shows that NC-FinFET SRAM cell exhibits larger hold static noise margin (HSNM) than FinFET SRAM cell due to its better subthreshold swing induced by negative capacitance effect. HSNM increases as T_{fe} increases. NC-FinFET SRAM cell with T_{FE} = 7nm shows superior HSNM which is nearly close to V_{DD}/2 line. Fig. 10 shows a hysteresis window (= 30mV) is observed of HSNM for NC-FinFET SRAM cell (T_{fe} = 7nm) at V_{DD} = 1V due to the NDR effect.

Acknowledgements

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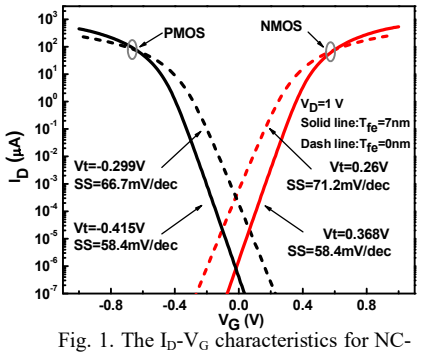

Fig. 1. The I_D-V_G characteristics for NC-FinFETs (T_{fe} = 7nm) and FinFETs (T_{fe} = 0nm) at V_D = 1V. NC-FinFETs show larger threshold voltage and better subthreshold swing than FinFETs.

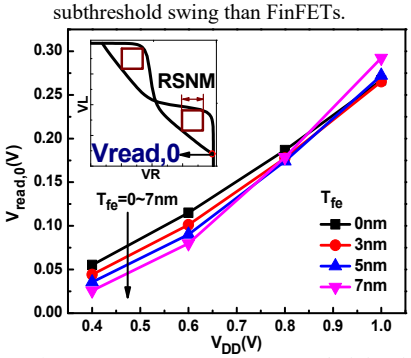

Fig. 4. At V_{DD} = 0.4V~ 0.6V (near-/subthreshold region), NC-FinFET SRAM cell shows lower read disturb voltage ($V_{read,0}$) than the FinFET SRAM cell due to improved subthreshold swing. The inset shows the definitions of RSNM and $V_{read,0}$. RSNM increases as $V_{read,0}$ decreases.

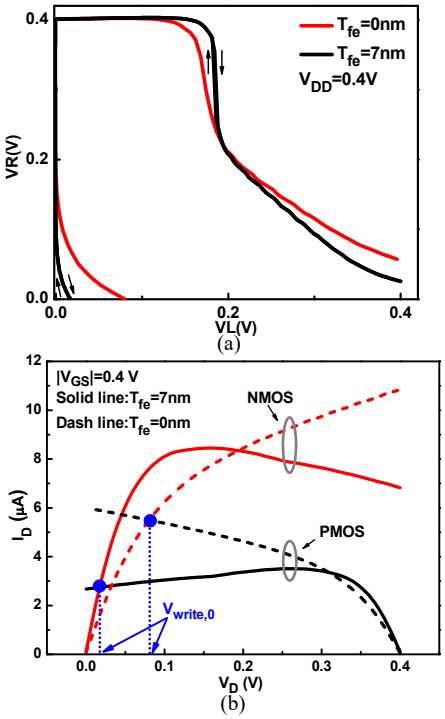

Fig. 7. (a) At V_{DD}= 0.4V, NC-FinFET SRAM cell with T_{fe} = 7nm shows larger WSNM and smaller $V_{write,0}$ than FinFET SRAM cell. (b) Pull-up PMOS and pass-gate NMOS load line analysis for NC-FinFET and FinFET SRAM cells during write operation, and the intersection of two load lines (blue circle) describes the $V_{write,0}$. At V_{DD} = 0.4V, pass-gate NMOS with negative capacitance effect becomes stronger, and pull-up PMOS with negative DIBL and negative differential resistance effect becomes weaker, and therefore NC-FinFET SRAM cell exhibits lower $V_{write,0}$.

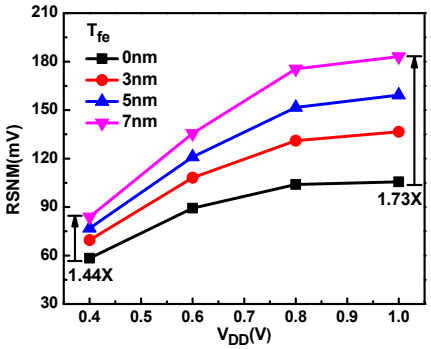

Fig. 2. The read static noise margin (RSNM) for 6T FinFET (T_{fe} = 0nm) and NC-FinFET (T_{fe} = 3nm~7nm) SRAM cells in the near-/sub-threshold and superthreshold regions. NC-FinFET (T_{fe}= 7nm) SRAM cell exhibits 1.73 times (1.44 times) larger RSNM than FinFET SRAM cell at V_{DD} = 1V (V_{DD} = 0.4V). As T_{fe} increases, RSNM of NC-FinFET SRAM cell increases.

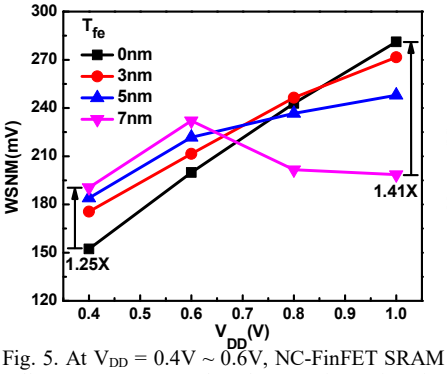

Fig. 5. At V_{DD} = 0.4V ~ 0.6V, NC-FinFET SRAM cells (T_{fe} = 3nm~7nm) show larger write static noise margin (WSNM) than the FinFET SRAM cell (T_{fe} = 0nm). At V_{DD} = 1V, NC-FinFET SRAM cells show lower WSNM than the FinFET SRAM cell, while NC-FinFET SRAM cell with T_{fe} = 7nm still exhibits adequate WSNM (= 198mV)

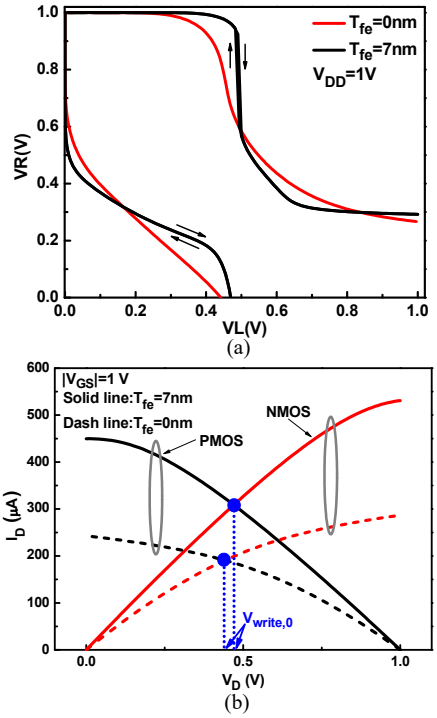

Fig. 8. (a) At V_{DD}=1V, NC-FinFET SRAM cell with T_{fe} = 7nm shows smaller WSNM and lager $V_{write,0}$ than FinFET SRAM cell. (b) NC-FinFETs exhibit larger drain saturation voltage [$V_{Dsat} = (V_G - V_t)/m$], and both pull-up and pass-gate devices operate in the linear region which increases the $V_{write,0}$ and decreases WSNM. Negligible hysteresis window of WSNM is observed for NC-FinFET SRAM cell.

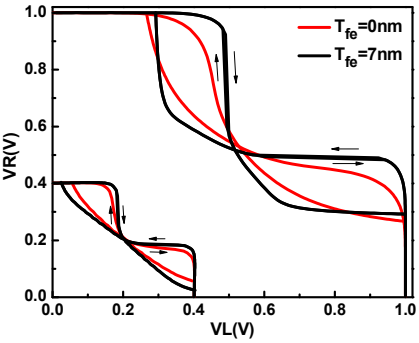

Fig. 3. The butterfly curves for determining the RSNM of NC-FinFET and FinFET SRAM cells in the near-/sub-threshold (V_{DD} = 0.4V) and superthreshold (V_{DD} = 1V) regions. NC-FinFETs show better RSNM. Negligible hysteresis window of RSNM is observed for NC-FinFETs SRAM cell at V_{DD} = 1V and 0.4V.

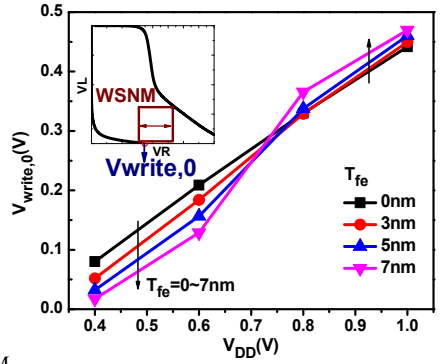

Fig. 6. NC-FinFETs SRAM cell with T_{fe} = 7nm exhibits larger $V_{write,0}$ at V_{DD} = 1V but smaller $V_{write,0}$ at V_{DD} = 0.4V~0.6V. The inset shows the definitions of WSNM and $V_{write,0}$. For SRAM cell, WSNM increases as $V_{write,0}$ decreases.

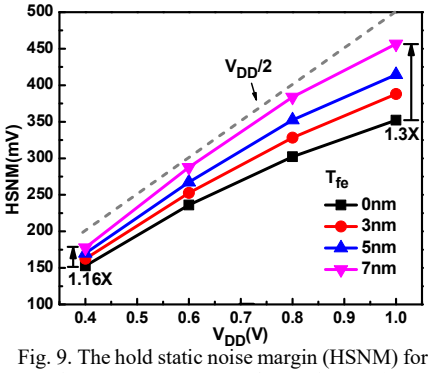

Fig. 9. The hold static noise margin (HSNM) for 6T FinFET (T_{fe} = 0nm) and NC-FinFET (T_{fe} = 3nm~7nm) SRAM cells in the near-/subthreshold and superthreshold regions. When T_{fe}=7nm, it shows superior HSNM and nearly close to the V_{DD}/2 line.

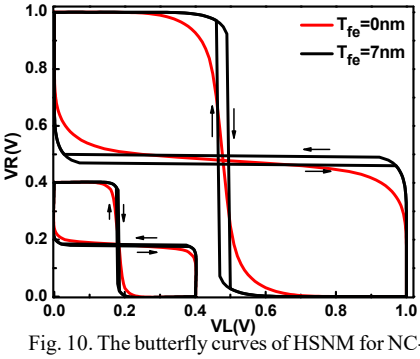

Fig. 10. The butterfly curves of HSNM for NC-FinFET and FinFET SRAM cells in the subthreshold and superthreshold regions. NC-FinFETs SRAM shows better HSNM at V_{DD} = 1V and 0.4V. At V_{DD} = 1V, hysteresis is observed for HSNM.