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Reliability of 60-nm scale CAAC-IGZO FET

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Abstract

The reliability of 60-nm scale field-effect transistors (FETs) using c-axis aligned crystalline indium-gallium-zinc oxide (CAAC-IGZO) in a channel region was evaluated through various reliability tests. As a result, such FETs had high reliability. One of the tests was a positive gate bias temperature (PGBT) test that applies stress at a gate voltage (V_g) of 2.75V and a temperature (T) of 150°C for 200 hours. This test result showed that the variation amount of threshold voltage until 200 hours was less than 100mV. Considering the temperature acceleration in PGBT degradation, the threshold voltage variation in PGBT test at 125°C and V_g=2.75V is estimated to be less than 100mV until 2000 or 2500 hours.

1. Introduction

Recently, FETs using CAAC-IGZO have been studied and applied to backplanes of liquid crystal and organic light-emitting diode displays [1]. CAAC-IGZO FET has high stability because of its crystallinity [2]. Another feature of this FET is extremely low off-state current [3], which has been utilized to drive displays with less power. In addition, low-power electronic devices such as a memory, an FPGA, a CPU are expected to be fabricated with use of CAAC-IGZO FETs. Although FETs at a micrometer scale are used in display devices, further scaling FETs are necessary in LSI devices. Therefore, several tens of nanometer-sized CAAC-IGZO FETs have been investigated [4-6]. For example, the FETs with trench gate self-aligned (TGSA) structure were reported [5,6]. FETs used in LSI devices need to have higher reliability than those used in display devices. This report shows reliability of 60-nm-scale CAAC-IGZO FETs.

2. Device Structure

A device structure we fabricated was a TGSA with some improvements from the conventional ones to have better characteristics and reliability. Figure 1 shows a schematic diagram of TGSA structure and cross-sectional STEM images in channel-length (L) and channel-width (W) directions. The FET size was W/L=60nm/60nm (designed value). A gate insulating film had a thickness of 6 nm. To improve the controllability of a gate electrode, the side surface of CAAC-IGZO was covered with the gate electrode. The IGZO FET is able to be fabricated as an interlayer in an LSI device. For example, the IGZO FET is fabricated over a circuit constructed with silicon-MOSFETs.

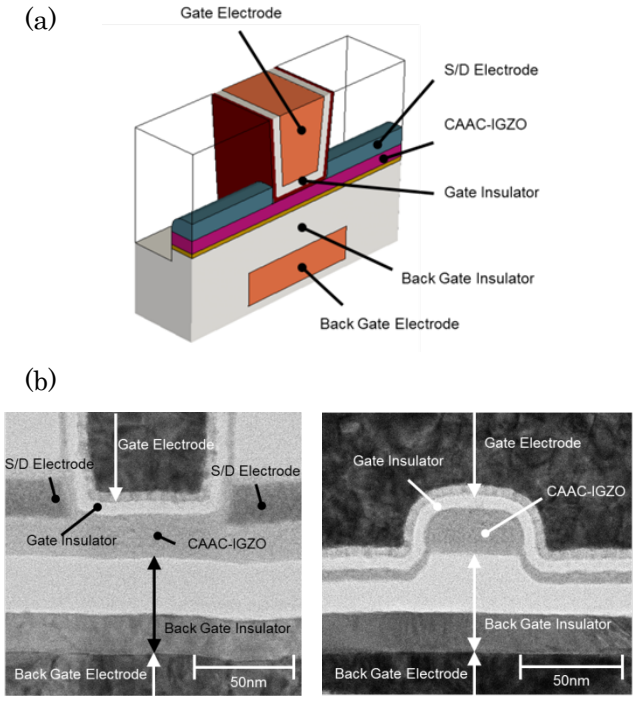

Fig.1 (a) Schematic diagram of TGSA structure and (b) Cross-sectional STEM images (left: L-direction, right: W-direction).

3. Reliability Evaluation

High reliability is required for CAAC-IGZO FETs in LSI devices. We examined the degradation amount through PGBT, negative GBT (NGBT), positive drain bias-temperature (PDBT), and positive drain GBT (PDGBT) tests as evaluation of reliability. The stress conditions were V_g=3.63V in PGBT, V_g=−1.32V in NGBT, V_d=1.32V in PDBT, and V_g=1.32V and V_d=3.63V in PDBGT, which were set assuming IGZO-FET application. The electrodes which are not mentioned above were applied with 0V. We define "V_{sh}" as the V_g value when I_d becomes equal to 10^{-12}A in the I_d-V_g characteristics at V_d=1.2V. The temperature was set to 125°C. Figure 2 shows results of these tests. The degradation amounts in PGBT, NGBT, and PDBT were small. Meanwhile, the degradation amount in PDGBT is large; however, the period of applying this stress is short in actual circuit operation.

Although 3.63V was applied as stress in our PGBT test as shown in Fig. 2, the operating voltage would be much lower because there is a demand on lowering the power supply voltage. We also conducted PGBT test with a stress voltage of 2.75V to examine a variation in characteristics. In

this test, the temperature was set to 150°C to accelerate degradation based on an experience showing that the drift degradation under PBT stress application is accelerated by approximately 10 to 13 times when the temperature is increased from 125°C to 150°C.

Figure 3 shows temporal variations in ΔV_{sh}, drain current I_d at V_g=2.5V, subthreshold swing (*SS*), linear field-effect mobility (μ_{FE}) during PGBT stress application. These values were derived from the I_d-V_g characteristics at V_d=1.2V and T=150℃. The variation in ΔV_{sh} until 200 hours was less than 100mV. Considering the temperature acceleration in PGBT, ΔV_{sh} at T=125°C is estimated to less than 100mV until 2000 or 2500 hours. Furthermore, I_d was slightly increased with negative drift of threshold voltage. Major changes in *SS* and μ_{FE} value were not observed.

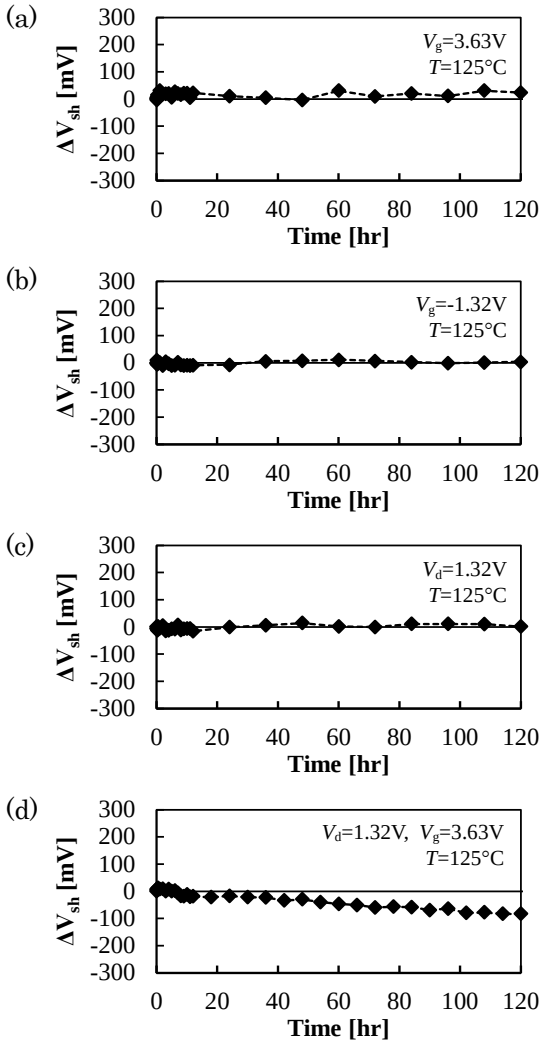

Fig.2 Temporal variation of ΔV_{sh} in (a) PGBT test, (b) NGBT test, (c) PDBT test, and (d) PDGBT test.

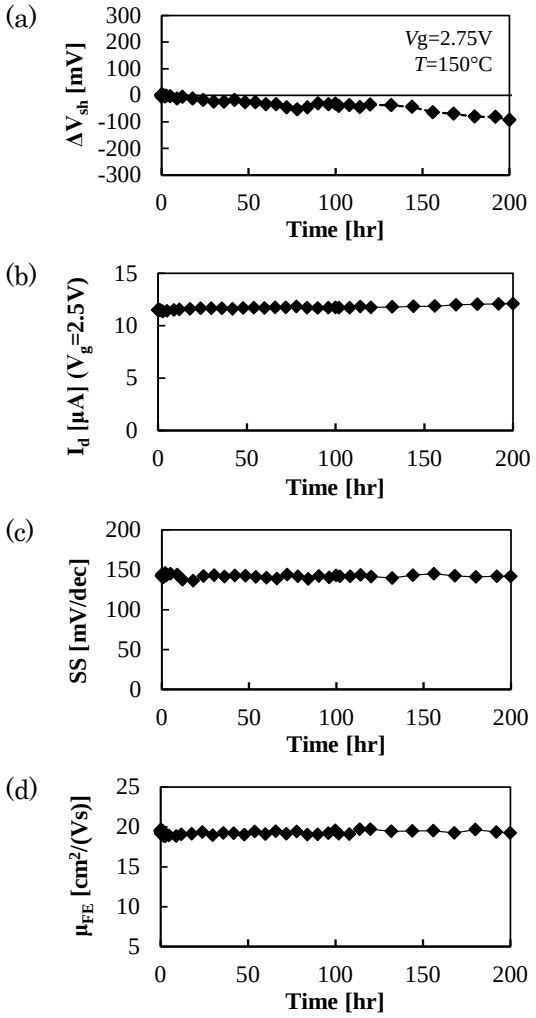

Fig.3 Temporal variation of (a) $\Delta V_{sh,}$ (b) I_d at V_g=2.5V, (c) *SS*, and (d) μ_{FE}, during PGBT stress application.

4. Conclusion

Reliability of 60-nm scale FETs using CAAC-IGZO as a channel material was evaluated. As the reliability test, we conducted a PGBT test with severe conditions for reliability at V_g=2.75V and T=150°C for 200 hours. The test result showed that the variation amount of threshold voltage until 200 hours was less than 100mV. According to the result, the threshold voltage variation in PGBT test at 125°C and V_g=2.75V is estimated to be less than 100mV until 2000 or 2500 hours in consideration of the temperature acceleration in PGBT degradation. The evaluation results indicate that our fabricated CAAC-IGZO FETs could have the commercial viability.

References

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