# Effect of Low Angle Grain Boundaries on Electron and Hole Mobility

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## Abstract

High performance perpendicular TFTs were achieved on (100) oriented poly-Si thin films with electron field effect mobility of 518 cm<sup>2</sup>/Vs. Their performance variation was high due to strong effect of cross grain boundaries and the difference of misorientation angles at grain boundaries. P-channel TFTs had low hole field effect mobility. The performance of parallel and perpendicular TFTs were insignificantly different.

## 1. Introduction

Bi-axially (100) oriented poly-Si thin films have been formed continuous-wave laser lateral crystallization. (100) textures have been formed in large areas by overlapping scanning process. In addition, ultrahigh-performance low temperature poly-Si thin film transistors with electron field effect mobility up to 1000 cm<sup>2</sup>/Vs fabricated on the (100) poly-Si films have been reported in our previous works[1,2]. These achievements are promising to develop Si electronics to a new page that high-speed glass sheet computers can be realized. In this work, we developed perpendicular n-channel TFTs and p-channel TFTs on (100)-oriented poly-Si thin films to investigate effect of low angle grain boundaries on electron and hole mobility.

## 2. Experimentals

LTPS-TFTs was fabricated as the same process as our previous work with maximal temperature of 550 °C[1]. As and B ion implantation was applied for n-channel TFTs (dose:  $2 \times 10^{15}$  cm<sup>-2</sup>, accelerating voltage: 13 kV) and p-channel TFTs (dose:  $2 \times 10^{15}$  cm<sup>-2</sup>, accelerating voltage: 13 kV), respectively. Figure 1 shows photomicrograph of typical fabricated TFTs.



Fig. 1 photomicrograph of typical fabricated TFTs.

### 2. Results and Discussions



Fig. 2  $I_{DS}$ - $V_{GS}$  characteristics of a typical perpendicular TFT.

Figure 2 shows drain current  $(I_{DS})$  versus gate voltages  $(V_{GS})$  characteristics of a typical fabricated perpendicular TFT with  $W = 10 \ \mu m$  and  $L = 10 \ \mu m$ . The TFT had ON/OFF current ratio of  $10^6$ , a threshold voltage ( $V_{th}$ ) of -0.8 V, and a sub-threshold slope (S) of 114 mV/dec. The curve of the electron field effect mobility ( $\mu_{FE}$ ) versus  $V_{GS}$  shows a mobility of 480 cm<sup>2</sup>/Vs. This mobility is twice smaller than that of parallel TFTs[1]. This result illustrates a strong effect of grain boundaries on the electron mobility. Crystal grains averagely had 2 µm width and 20 µm length. Contrary to parallel TFTs, perpendicular TFTs had grain boundaries crossed the current flow of 10  $\mu$ m length channels. These crossed grain boundaries induced barrier potentials and reduced the mobility. The misorientation angles of the grain boundaries between (100) crystals were small. They induced few grain boundary trap states, few donor concentrations, and insignificant grain boudaries scattering. Therefore the TFT had a small subthreshold slope and a low leakage current.

 Table 1 average performances and their variations of perpendicular TFTs

Maximum Mobility $\mu_{FE}$ (cm <sup>-2</sup> V <sup>-1</sup> s <sup>-1</sup> )	518
Average mobility $\mu_{FE}$ (cm <sup>-2</sup> V <sup>-1</sup> s <sup>-1</sup> )	$329\pm112$
Subthreshold slope (S) (mV/dec)	$517\pm344$
ON/OFF ratio	$10^{2} \div 10^{8}$
Threshold voltage Vth (V)	$-1.3 \pm 0.3$

As a result of a strong grain boundary effect, the perpendicular TFTs had a low average performance and high variation, as shown in table 1. The average electron mobility of perpendicular TFTs of (100) poly-Si thin films was twice lower than that of parallel TFTs. Their average subthreshold slope and its variation was also higher.



Fig. 3  $I_{DS}$ - $V_{GS}$  and  $I_{DS}$ - $V_{DS}$  characteristics of a typical parallel p-channel TFT.

Figure 3 shows drain current ( $I_{DS}$ ) versus gate voltages ( $V_{GS}$ ) of a typical fabricated parallel p-channel TFT with a same channel size with n-channel TFTs ( $W = 10 \ \mu$ m and  $L = 10 \ \mu$ m). The  $I_{DS}$ - $V_{GS}$  relationship at  $V_{DS} = 0.5$  V on an exponential scale indicated an ON/OFF current ratio of 10<sup>6</sup>, a threshold voltage ( $V_{th}$ ) of -0.4 V, and a sub-threshold slope (S) of 0.14 V/dec. The curve of the hole field effect mobility ( $\mu_{FE}$ ) versus  $V_{GS}$  shows the hole mobility of 146 cm<sup>2</sup>/Vs. This mobility is extremely lower than the electron mobility.



Fig. 4  $I_{DS}$ - $V_{GS}$  characteristics of a typical perpendicular p-channel TFT.

Figure 4 shows  $I_{DS}$ - $V_{GS}$  characteristics of a typical perpendicular p-channel TFT with the same channel size with parallel TFTs ( $W = 10 \ \mu m$  and  $L = 10 \ \mu m$ ). It appears that characteristics of parallel and perpendicular TFTs were similar. They had an almost same hole mobility, subthreshold

slope, ON/OFF ratio, and threshold voltage.

**Table 2** Average performance and its variation of parallel p-channel TFTs ( $W = 3 \mu m$ ,  $L = 10 \mu m$ )

Maximum Mobility $\mu_{FE}$ (cm <sup>-2</sup> V <sup>-1</sup> s <sup>-1</sup> )	230
Average mobility $\mu_{FE}$ (cm <sup>-2</sup> V <sup>-1</sup> s <sup>-1</sup> )	$148 \pm 46$
Subthreshold slope (S) (mV/dec)	$117 \pm 21$
ON/OFF ratio	$10^{5}$ - $10^{6}$
Threshold voltage <i>Vth</i> (V)	$0.3 \pm 0.2$

The p-channel TFTs with  $W = 3 \mu m$  had better characteristics than others. Their average performances and their variation are summarized in Tab. 2. It is found that their average hole mobility was low and its deviation was large. However, they had good threshold slope and high ON/OFF ratio. The highest hole mobility of 230 cm<sup>-2</sup>V<sup>-1</sup>s<sup>-1</sup> was realized. This mobility was similar to that in the previous report of A. Hara et al. [3].

## 4. Conclusions

High performance perpendicular TFTs were achieved on (100) oriented poly-Si thin films. They had maximal electron field effect mobility of 518 cm<sup>2</sup>/Vs. This mobility was twice smaller than that of parallel TFTs. However, their performance variation was higher than that of parallel TFTs due to strong effect of cross grain boundaries and the difference of misorientation angles at grain boundaries. P-channel TFTs were also fabricated on (100) poly-Si thin film. The characteristics of p-channel TFTs seem to be contrary with n-channel TFTs. They had very low hole field effect mobility that was much smaller than electron mobility. In addition, the mobilities of parallel and perpendicular TFTs were insignificantly different.

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## References

[1] T. T. Nguyen, M. Hiraiwa, and S.-I. Kuroki, Appl. Phys. Exp., **10**, 056501 (2017).

[2] T. T. Nguyen, M. Hiraiwa, T. Hirata, and S.-I Kuroki, ECS Transactions, **75**(10), 49-54 (2016).

[3] A. Hara, M. Takei, F. Takeuchi, K. Suga, K. Yoshino, M. Chida, T. Kakehi, Y. Ebiko, Y. Sano, and N. Sasaki, Jpn. J. Appl. Phys. **43**, 1269 (2004).