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Wafer-Level-Probing Electrical Properties of Planar Junctionless Poly-Si Thin-Film Transistors Using a Novel C-V Charcacterization Scheme

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Abstract

We reported electrical parameters, including gate oxide thickness (T_{ox}), channel carrier concentration (n), and fixed charge density (Q_f), of N-type junctionless (JL) planar poly-Si thin-film transistors (TFTs) as well as their distribution uniformity on a six-inch wafer probed with a novel C-V characterization method. Values of n and Q_f in the orders of 10^{19}cm^{-3} and 10^{12} cm^{-2}, respectively, are recorded. Polarity of Q_f is found to be negative owing to the P segregation at the oxide/channel interface. Moreover, bull's eye effect for the Q_f distribution is clearly observed.

1. Introduction

Junctionless (JL) transistors are merited for their simple device structure and the ease of fabrication complexity due to the elimination of *p*-*n* S/D junctions [1, 2]. Thereby, we are able to produce poly-Si JL transistors [3, 4] on an insulating substrate at low thermal budgets, enabling their feasibility for the construction of 3D electronics. Previously, we have fabricated poly-Si planar TFTs [3] and nanowire transistors [4] of *in situ* P-doped poly-Si channels with good device performance, verifying their great potentials for practical applications. We have also proposed a novel capacitance-voltage (C-V) characterization technique to extract major electrical parameters of interfacial fixed charge density (Q_f) and carrier concentration (n) for planar JL devices [3]. In this work, we further advanced this C-V technique to probe the uniformity of the electrical properties for the poly-Si JL TFTs fabricated on a 6" Si wafer.

2. Device Structures and C-V Characterization Scheme

Fig. 1 depicts the studied device structure. Details of the fabrication process for the test devices have been described elsewhere [3]. In this work, the gate stack of the tested devices comprises of a 12nm-thick *in situ* phosphorous-doped poly-Si channel layer deposited by LPCVD, a nominal 9nm-thick gate oxide of SiO_2, and an n^+ poly-Si gate. To precisely measure the capacitance of the intrinsic channel, we measured two devices with various channel areas of $L\times W$ = 20μm/100μm and 50μm/100μm but having identical source/drain pads and then normalize the capacitance difference between the two devices by the difference of the channel areas. In this scheme, the primary formulas for the extraction of important electrical parameters of flat-band voltage (V_{FB}) and depletion width (X_{dep}) are summarized in Table I. The measured data (e.g., Figs. 2 and 3) can be divided into two regions (denoted as I and II). For Region I ($V_G > V_{FB}$), the formation of an accumulation channel layer set the measured capacitance equal to the gate-oxide capacitance. On the other hand, the depletion capacitance must be taken into account for the measured capacitance in Region II where $V_G < V_{FB}$. Thereby, we are able to determine V_{FB} directly from the measured capacitance data. In addition, the C-V data near V_{FB} can be fitted by equations (1) and (3) in Table I, and then we are able to extract the gate oxide thickness (T_{ox}), n, and even Q_f from Eq. (2) once n being extracted.

3. Results and Discussion

To gain insights on the uniformity of electrical characteristics for our poly-Si JL TFTs, we have conducted wafer-level C-V measurements on transistors located in various dies on a 6-inch wafer. Typical C-V results measured on an edge die and a central die are shown in Figs. 2 and 3, respectively. Table II summarizes major electrical parameters extracted from the two figures. It is seen that the extracted gate-oxide thicknesses is very close to the nominal value of 9nm. The extracted electron concentration in the channel is approximate 2×10^{19} cm^{-3} in magnitude, which is consistent with the previous reported data [3]. Another interesting findings for our poly-Si JL TFTs from this extraction are the existence of negative fixed charges, which has been attributable to P segregation at the gate oxide/channel interface [5], as well as the measured Q_f of -2.52×10^{12} cm^{-2} for the device at the central die tending to be larger than the one (-2.17×10^{12} cm^{-2}) at the edge.

The wafer-level mapping of Q_f shown in Fig.4 further strengthens the "bull's-eye" distribution, *i.e.*, the Q_f values peak at the central dies and then radially decreases for the dies at the outer rings. This is reminiscent of the "bull's eye" effect commonly observed in the films deposited using LPCVD systems [6][7], which is probably caused by the high reactivity of the gas-phase products. [6]. Exploration of the origins for such a distribution is still in progress. The variations in Q_f lead to a shift in the threshold voltage (V_{th}), as shown in Figs. 5 and 6. Once again, a bull's-eye distribution pattern is observed for the wafer-level mapping of V_{th} as shown in Fig. 6.

4. Conclusions

Using a novel C-V probing scheme we report the wafer-level mapping of major electrical parameters, including channel carrier concentration, fixed charges, and V_{th}, for planar JL poly-Si TFTs that were fabricated on a six-inch Si wafer. An interesting finding from the wafer-level maps of these electrical parameters is that all the studied electrical parameters

show bull's eye distributions. The valuable information can be fed back to process engineers to modify the deposition conditions or to refine the deposition system design for uniformity improvements.

Acknowledgement

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References

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Table I Formulas derived in the C-V characterization scheme for extraction of the electrical parameters of the JL TFTs.

Region I ($V_G \geq V_{FB}$)	**Region II** ($V_G < V_{FB}$)
$C = C_{ox}$ (1)	$C = \left(\frac{1}{C_{ox}} + \frac{1}{C_{dep}}\right)^{-1}$ (3)
$V_{FB} = -\left(\frac{E_g}{2} - \frac{kT}{q} ln\left(\frac{n}{n_i}\right)\right) - \frac{Q_f}{C_{ox}}$ (2)	$C_{dep} = \frac{\epsilon_{si}}{X_{dep}}$ (4)
	$X_{dep} = -\frac{\epsilon_{si}}{C_{ox}} + \sqrt{(\frac{\epsilon_{si}}{C_{ox}})^2 - \frac{2\epsilon_{si}(V_G - V_{FB})}{qn}}$ (5)

C_{ox}: oxide capacitance per unit area; ϵ_{Si}: permittivity of Si
C_{dep}: capacitance of channel depletion region per unit area;
X_{dep}: thickness of channel depletion region; E_g: bandgap of Si

Table II Major parameters extracted from the C-V results present in Fig.2 and Fig.3.

Parameters	Center	Edge
Gate oxide thickness, T_{ox} (nm)	8.7	9.1
Carrier concentration, n (10^{19} cm^{-2})	2.09	2.33
Flat-band voltage, V_{FB} (V)	1.1	0.9
Fixed charge density, Q_f/q (10^{12} cm^{-2})	-2.52	-2.17

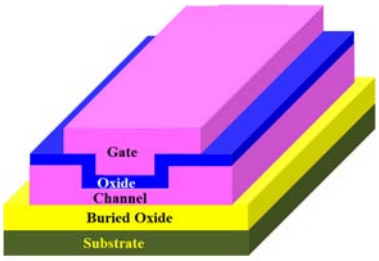

Fig. 1 Schematic illustration of the planar poly-Si JL TFTs.

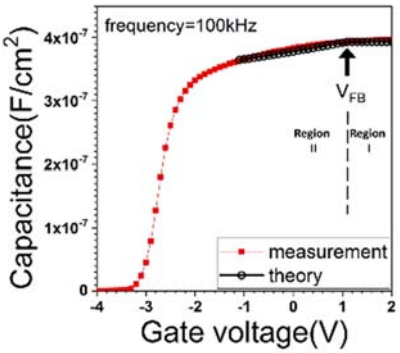

Fig. 2 Typical C-V characteristics obtained from testers located in an edge die.

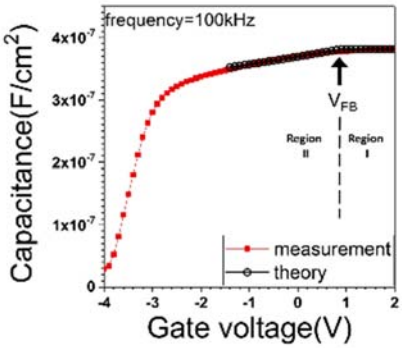

Fig. 3 Typical C-V characteristics obtained from testers located in a central die.

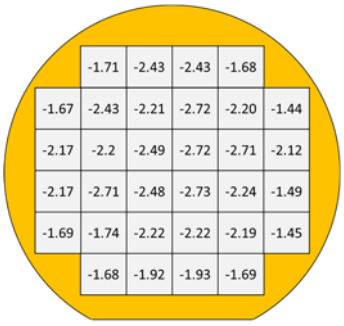

Fig. 4 Mapping plot of Q_f/q (x10^{12}cm^{-2}) measured from testers of different dies on a six-inch Si wafer.

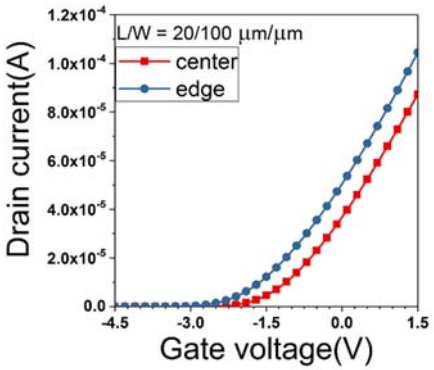

Fig. 5 Transfer characteristics of the transistors (L/W = 20/100 μm/μm) characterized in Figs. 2 and 3.

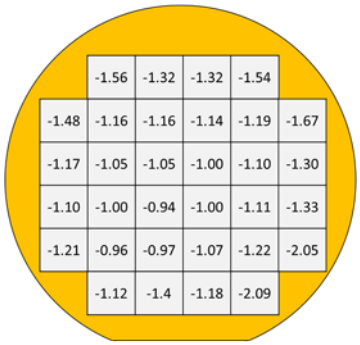

Fig. 6 Mapping plot of V_{th} (in V) measured from transistors (L/W = 20/100 μm/μm) of different dies on a six-inch Si wafer.