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Stacked Source/Drain Electrode Structure of InGaZnO Thin-Film-Transistor for Low Contact Resistance and Suppressing Channel Shortening Effect

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Abstract

Reduction of Source/Drain (S/D) parasitic resistance with suppressing effective channel length (L_{eff}) shortening after high temperature process is key to realize for integrating high performance short channel InGaZnO Thin-Film-Transistors (TFT) to 3D-LSIs. In order to achieve this requirement, we propose a stacked source/drain electrode structure of a metal thin film and In-Sn-O (ITO). By inserting the metal thin film between InGaZnO channel and ITO electrode, about 11 times improvement of on-current, I_{on} (I_d @V_g = 20V, V_d = 50 mV) was achieved. Moreover, L_{eff} shortening were also suppressed even after 360°C annealing.

(Keywords: InGaZnO, stacked S/D electrode structure)

Introduction

Recently, InGaZnO TFT has much attracted attention as high performance BEOL transistors for 3D-LSIs, because InGaZnO TFT can be fabricated below 400 °C process and show a mobility of around 10 cm^2/Vs[1-3]. On the other hands, InGaZnO TFT, especially for short channel device, suffers from the L_{eff} shortening caused by the formation of the oxygen vacancies in InGaZnO channel, generated by the reduction reaction between S/D electrode and InGaZnO [4, 5]. Previously, we have reported the suppression effect of the channel shortening effect by using ITO S/D electrode [6]. However, the InGaZnO TFT with ITO electrode exhibits I_{on} degradation compared to the InGaZnO TFT with Ti electrode, due to the higher contact resistance ($R_{contact}$) at the InGaZnO/ITO interface. In order to suppress this I_{on} degradation, we have been proposed the stacked S/D electrode structure of InGaZnO/W thin film/ITO and successfully demonstrate the I_{on} improvement with suppressing L_{eff} shortening.

TFT fabrication

Figure 1 shows the concept of proposed stacked S/D electrode structure. By inserting the W thin film at the InGaZnO/ITO interface, carrier concentrations of InGaZnO near the ITO are increased due to the formation of the oxygen vacancies in InGaZnO channel generated by the reduction reaction between W and InGaZnO. As a result, the width of the depletion layer between ITO and InGaZnO is thinned and $R_{contact}$ of InGaZnO/ITO is expected to be decreased, accordingly, R_{para} also decreases. Since the inserted W is thin enough, the reduction reaction of InGaZnO restricted only near the S/D electrode. Therefore, L_{eff} shortening can be effectively suppressed. We fabricated the TFTs as shown in Fig. 2. A 40nm-SiO_2 was used as a gate insulator and a 15nm-thick InGaZnO was used as a channel. A 30nm-thick ITO was used as the S/D electrode. Here, W thin film was inserted between InGaZnO and ITO. The channel lengths, L_g were prepared in the range from 0.8μm to 5.0μm, and the channel widths, W were 1.4μm and 2.4μm, respectively. Figure 3 shows the cross sectional transmission electron microscope (TEM) images of the S/D structure. About 2nm W was clearly observed between InGaZnO and ITO with W/ITO electrode sample.

Experimental results and discussions

Figure 4 shows the I_d-V_g characteristics of InGaZnO TFTs. The TFT with W/ITO electrode obtained 11 times higher I_{on} than that of the TFT with ITO electrode. Figure 5 shows the I_d-V_d characteristics of InGaZnO TFTs. The I_d-V_d curves showed Schottky like behavior with ITO electrode case. On the other hands, with W/ITO electrode case, I_d-V_d curves exhibited better ohmic characteristics at the low V_d conditions. Figure 6 shows the on-resistance (R_{on}) -gate length (L_g) plot. The parasitic resistance (R_{para}) of InGaZnO TFTs was extracted from the R_{on}-L_g plot. The intersection of the extrapolated line and Y-axis corresponds to R_{para}. Figure 7 shows the gate overdrive voltage (V_g - V_{th}) dependence of R_{para} of InGaZnO TFTs. R_{para} of the TFT with W/ITO electrode were decreased about 94 % compared to R_{para} of the TFT with ITO electrode. These results indicate that good ohmic contact is formed between InGaZnO and ITO by inserting W at the InGaZnO/ITO interface. In order to understand the mechanism of this I_{on} improvement of the TFT with W/ITO electrode, X-ray photoelectron spectroscopy (XPS) analysis was carried out. For XPS analysis, the multilayer of InGaZnO/ITO and InGaZnO/W/ITO were deposited on a thermal oxidized Si wafer with the same thickness and condition of the TFT devices. Figure 8 shows the In and Ga spectra of InGaZnO at the InGaZnO/ITO interface. With ITO electrode case, only one peak originated from the metal oxide (In-O, Ga-O) was observed. Contrary, with W/ITO electrode case, two peaks originated from the metal oxide and the oxygen deficiency were observed. These results indicate that the oxygen vacancies were formed in InGaZnO by the reduction reaction between W and InGaZnO. From the electrical characteristics and XPS analysis, we propose the following model of the I_{on} improvement of the TFT with W/ITO electrode. The carrier concentrations of InGaZnO near ITO are increased by the reduction reaction of W and InGaZnO. As a result, the width of the depletion layer between InGaZnO/ITO is thinned and tunneling electron increased, hence R_{para} of InGaZnO TFT is decreased. Therefore, the TFT with W/ITO electrode exhibits higher I_{on} than that of the TFT with ITO electrode. Figure 9 shows the I_d-V_d characteristics of InGaZnO TFTs after 360°C annealing. About 7 times higher I_d (@V_g-V_{th}=6V) was obtained with the W/ITO electrode TFT compared to the ITO electrode TFT. The I_{on} improvement obtained by using W/ITO electrode was effective even after high temperature annealing. Moreover, in order to evaluate the L_{eff} of the InGaZnO TFTs after high temperature annealing, scanning spreading resistance microscopy (SSRM) measurements were performed. SSRM can visualize the resistance distribution in InGaZnO channel. For SSRM measurement, 100nm-thick InGaZnO was deposited on a thermally oxidized Si wafer. Then a 200nm-thick interlayer SiO_2 was deposited and patterned by RIE process. After that, a 100nm-thick ITO or W/ITO electrode was deposited. In order to evaluate L_{eff} shortening at accelerated test conditions, these samples were annealed at 400°C for 1h in N_2 ambient. Figure 10 shows the resistance distribution measured by SSRM. In the case of L_{eff} of InGaZnO TFT becomes shorter, the low-resistivity region extending to the lateral direction in InGaZnO channel from the S/D electrode is observed as shown in Fig. 10(a)[6]. In the case of (b) ITO, (c) W/ITO electrode, the uniform high resistance distribution to the lateral direction in InGaZnO channel was observed. This result indicates that W thin film inserted at the InGaZnO/ITO interface is not expanding the low resistivity region in InGaZnO channel even after 400°C annealing. Figure 11 shows the relationship between R_{para} and ΔL (ΔL is defined as the half length of the difference between L_g and L_{eff}) after 360 °C annealing. Here, ΔL is extracted from the $L_{overlap}$ dependence of I_d-V_g characteristics of the InGaZnO TFTs [6]. The ΔL was extended over 100nm after 360°C annealing with metal electrode such as Ti or W case. Contrary, the TFTs with W/ITO electrode could suppress the extension of the ΔL less than 40nm even after 360°C annealing. In addition, by using W/ITO electrode, R_{para} was decreased about 85% compared to the TFT with ITO electrode.

Conclusions

Improvement of the parasitic resistance with suppressing channel shortening effect for InGaZnO TFT has been demonstrated by using stacked S/D electrode of W thin film/ITO. The TFT with W/ITO electrode exhibits about 94% reductions of the parasitic resistance and about 11 times increase of the on-current compared to the ITO electrode TFT. Moreover, the low-resistivity region in InGaZnO channel was suppressed less than 40nm after 360°C annealing. These results indicate that the proposed stacked S/D electrode structure is effective for improving the parasitic resistance with suppressing channel shortening for InGaZnO TFT even after high temperature annealing.

References [1] K. Nomura et al., Nature, 432, 488(2004), [2] S. Jeon et al., IEDM 2010, p504, [3] Y. Kobayashi et al., VLSI 2014, p170, [4] H. Kitakado et al., JJAP. 51(2012) 03CB02., [5] S.H. Choi et al., IEEE ELECTRON DEVICE LETTERS, vol.35, no.8, p835 (2014), [6]J. Kataoka et al., EDTM 2018, p175

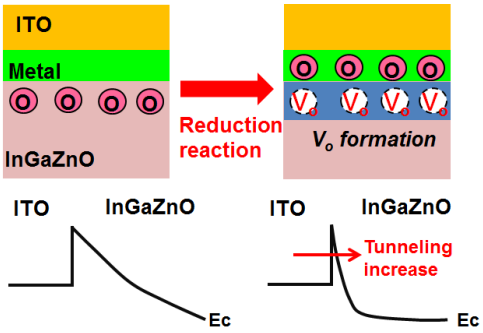

Fig.1 Concept of improving drain current for InGaZnO TFT.

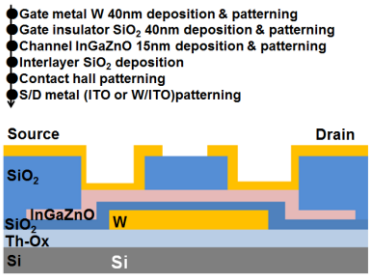

Fig.2 The schematic of fabricated InGaZnO TFTs.

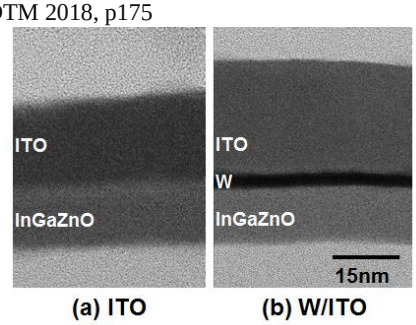

Fig.3 TEM images at the (a) InGaZnO/ITO, (b) InGaZnO/W/ITO interface. About 2nm-thick W was inserted between InGaZnO and ITO.

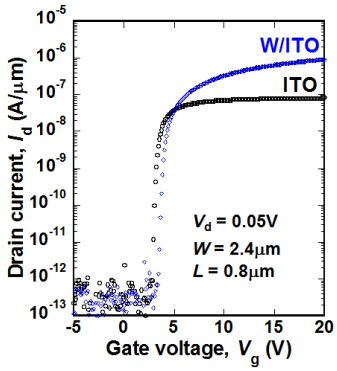

Fig.4 I_d-V_g characteristics of InGaZnO TFTs.

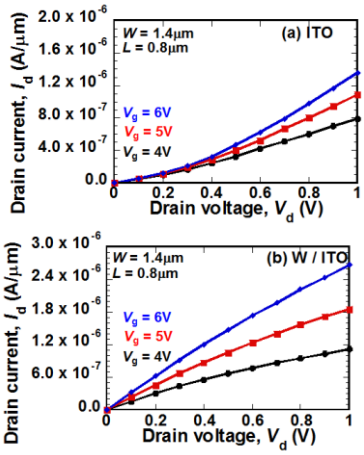

Fig.5 I_d-V_d characteristics of InGaZnO TFTs with (a) ITO, (b) W/ITO electrode.

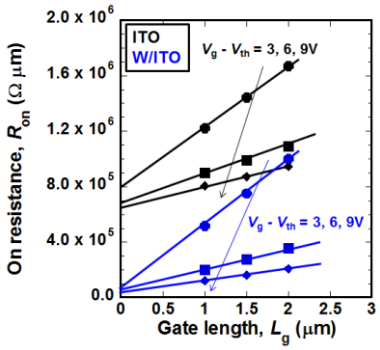

Fig.6 R_{on}-L_g plot of InGaZnO TFTs.

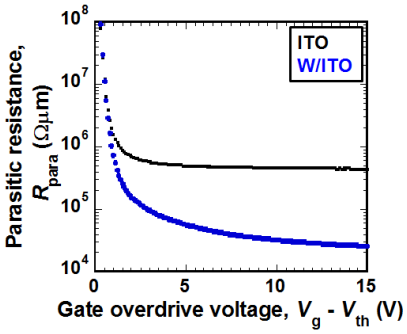

Fig.7 The gate overdrive voltage dependence of the parasitic resistance of InGaZnO TFT before annealing, extracted by R_{on}-L_g plot.

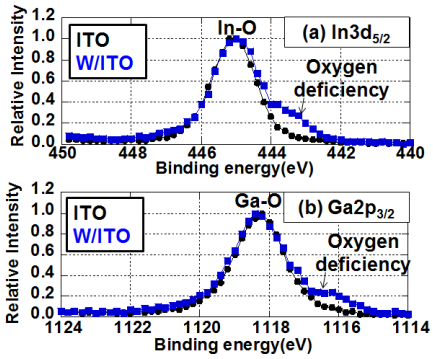

Fig.8 (a) In, (b) Ga spectra of InGaZnO at the InGaZnO/ITO interface measured by XPS.

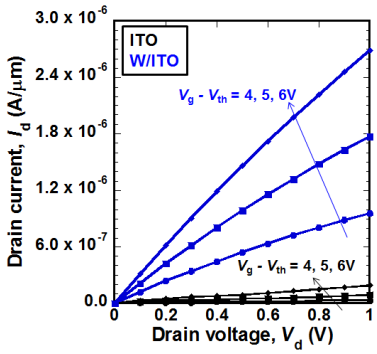

Fig.9 I_d-V_d characteristics of InGaZnO TFTs after 360°C annealing.

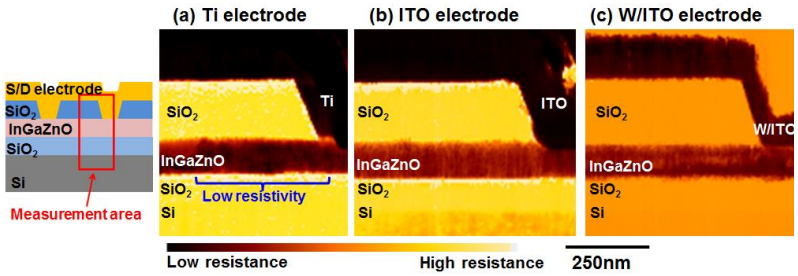

Fig.10 Resistance distribution of InGaZnO TFT with (a) Ti, (b) ITO, (c) W/ITO electrode after 400°C annealing measured by SSRM.

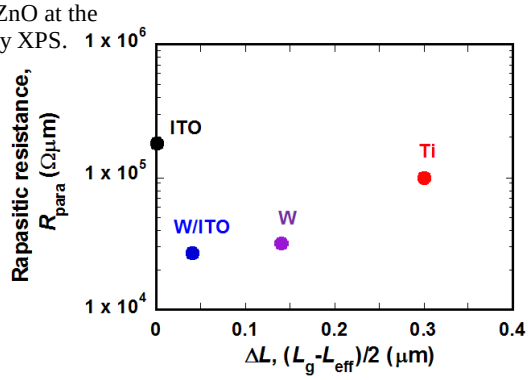

Fig.11 Relationship between R_{para} and ΔL of InGaZnO TFTs with various electrodes after 360°C annealing.