

Current Driven Macro-model of Phase-Change Material (PCM) Device Used for H-spice Simulation

Cheng Li¹, Juntae Choi¹, and Yun-Heub Song^{1*}

¹ Department of Electronics and Computer Engineering,
Hanyang University, Seoul 04763, Korea

* E-mail: yhsong2008@hanyang.ac.kr

Abstract

In this paper, we proposed a current driven macro-model of phase-change material (PCM) device using Verilog-A language for H-spice simulation. This model considers the three states during programming process: crystalline, amorphous, and melting state. The SET operation of this model is performed based-on the temperature dependent crystallization velocity. The RESET operation is realized based-on both internal temperature gradient of PCM device and the re-crystallize process with long falling time of programming pulse.

1. Introduction

The phase change memories are being studied as a candidate for next generation non-volatile memory, with its good properties such as multi-level resistance values, strong data retention, high endurance, promising reliability, CMOS compatibility, and technological maturity [1]. However, it is difficult for circuit design about phase-change random access memory (PRAM) circuits without a PCM device micro-model for H-spice simulation. In this paper, we proposed a current driven macro-model of PCM device using Verilog-A language, realizing the programming operation of PCM such as fully SET, partially SET, fully RESET, partially RESET and the programming dependent on falling time of pulse.

2. States and Operations of PCM Device

During the programming process, the PCM shows three states: crystalline, amorphous, and melting state. The resistance of PCM device (R_{PCM}) can be seen as the combination of these states (as shown in fig.1a) and the equation can be written as eq. (1):

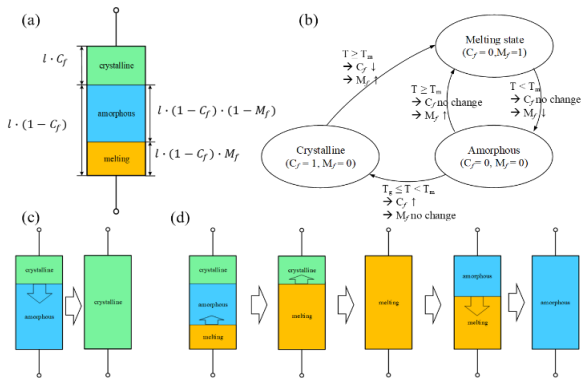


Fig. 1 (a) The PCM device is consisted of three states. (b) phase-change process between the three states. (c) SET operation (d) RESET operation

$$R_{PCM} = R_c \cdot C_f + R_a(1 - C_f)(1 - M_f) + R_m(1 - C_f)M_f \quad (1)$$

Here, R_c , R_a and R_m are the resistance of PCM device at fully crystalline state, fully amorphous state and fully melting state, and C_f and M_f are the crystalline fraction and the melting fraction, respectively. The R_{PCM} changes following the increasing or decreasing of C_f and M_f at certain temperature, as shown in fig.1b. If the temperature is below the crystallization trigger temperature (T_g), the PCM device remains its initial state. If the temperature is between T_g and the melting point (T_m), the SET operation is performed with increasing crystalline region as shown in fig.1c. The RESET operation requires the temperature above T_m and following a fast quenching process. As a result, the melting region increases firstly, and subsequently transfers into amorphous region during the quenching process, as shown in fig.1d. It should be pointed out that if falling time of programming pulse is long, the PCM device can be re-crystallized during the slow quenching process.

3. Module of PCM model

The proposed macro-model is consisted of circuit module and calculation module, as shown in fig.2a. A variable resistor is used to represent the PCM resistance. The calculation module is designed with four kinds of basic devices: resistor, capacitor, current source and voltage source. The calculation module includes temperature calculation module, C_f and M_f calculation module, and R_{PCM} calculation module. Fig.2b shows the performance of the model. Firstly, the calculation module receives the voltage of device (V_{PCM}) and R_{PCM} to calculate the cell temperature (T_{cell}) using temperature calculation module. Then C_f and M_f change according to the T_{cell} .

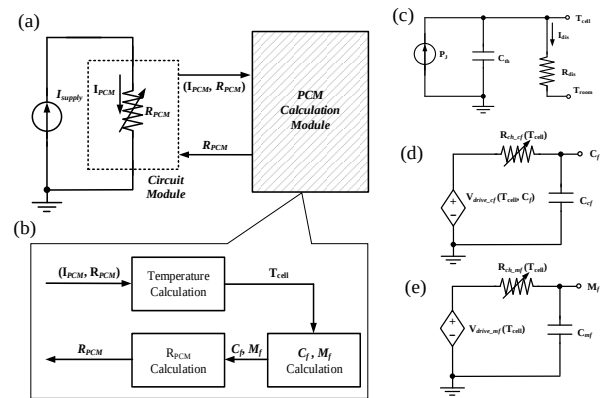


Fig. 2 (a) Modules of PCM device (b) Calculation module (c) Temperature calculation module (d) C_f calculation module (e) M_f calculation module

Finally, a new value of R_{PCM} is calculated using eq. (1) and send to the circuit module. The widely used temperature calculation module (fig.2c) is analyzed in [2]-[4]. The current source provides the quantity of heat from joule heating (P_j) according to the programming current and R_{PCM} . The resistor (R_{dis}) and capacitor (C_{th}) are used to simulate the thermal dissipation resistance and the thermal capability, respectively. The temperature is calculated using eq. (2) and eq. (3):

$$T_{cell} = \int \frac{P_j - I_{dis}}{C_{th}} dt \quad (2)$$

$$I_{dis} = \frac{T_{cell} - T_{room}}{R_{dis}} \quad (3)$$

The C_f and M_f calculation module are consisted of a capacitor, a variable resistor and a voltage source (as shown in fig.2d and fig.2e). The RC circuit can be used to control the crystallization velocity and melting velocity, whose equations are shown in [5]-[6]. The voltage sources drive C_f and M_f into the final results according to the cell temperature as eq. (4) and eq. (5):

$$V_{drive_cf}(T_{cell}, C_f) = \begin{cases} C_f, & \text{when } T_{cell} < T_g \\ 1, & \text{when } T_g \leq T_{cell} < T_m \\ 0, & \text{when } T_{cell} \geq T_m \end{cases} \quad (4)$$

$$V_{drive_mf}(T_{cell}) = \begin{cases} 0, & \text{when } T_{cell} < T_m \\ 1, & \text{when } T_{cell} \geq T_m \end{cases} \quad (5)$$

4. Simulation Result

The macro-model parameters are shown in Table. I. Typical programming current for fully SET and fully RESET are set as 15uA and 30uA, respectively. Fig.3 shows the simulation result of fully SET, fully RESET and the falling time de-

Table. I Macro-model Parameters		
Symbol	Value	Description
R_a	10M Ω	PCM resistance at fully amorphous state
R_c	100k Ω	PCM resistance at fully crystalline state
R_m	10k Ω	PCM resistance at fully melting state
T_g	400K	Crystallization trigger temperature
T_c	800K	Temperature with the fastest crystallization velocity
T_m	900K	Melting temperature

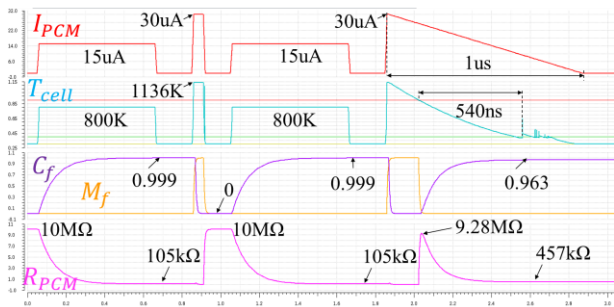


Fig. 3 Simulation result of fully SET, fully RESET and RESET operation dependent on falling time of pulse.

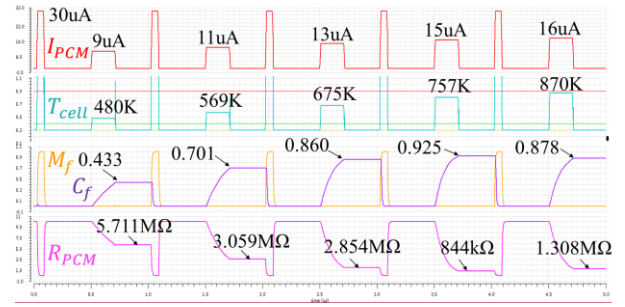


Fig. 4 Simulation result of SET operations

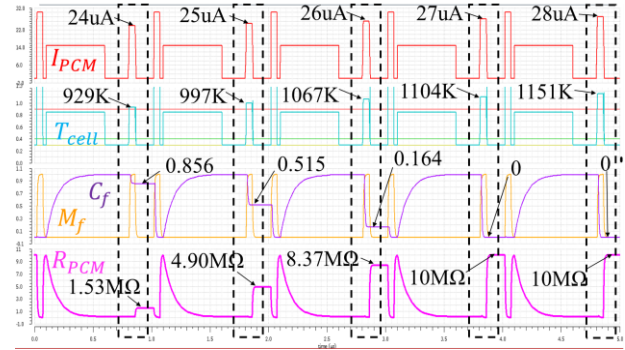


Fig. 5 Simulation result of RESET operations dependent on pulse amplitude

pendence of RESET operation. Fig.4 and fig.5 show the simulation results of the partially SET and partially RESET operations according to the pulse amplitude, respectively.

5. Conclusions

This research was supported by Nano Material Technology Development Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Science, ICT and Future Planning (NRF-2016M3A7B4910398).

Acknowledgements

The authors would like to thank K.W. Song and J.M. Baek of the Flash design team, Memory Division, Samsung Electronics Co., Ltd. for his support and helpful discussion. This research was supported by Nano Material Technology Development Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Science, ICT and Future Planning (NRF-2016M3A7B4910398).

References

- [1] HSP Wong et al., Proceedings of the IEEE, Volume 98, Issue 12, (2010) 2201-2227
- [2] K. C. Kwong, IEEE Trans. Electron Devices 55 (2008) 1672-1681
- [3] K. Sonoda et al., IEEE Trans. Electron Devices 55 (2008) 1672-1681
- [4] Manuel Le Gallo et al., Journal of Applied Physics 119, 025704 (2016)
- [5] S. Senkader, and C. D. Wright, JOURNAL OF APPLIED PHYSICS VOLUME 95, NUMBER 2 15 JANUARY 2004
- [6] Abu Sebastian, Manuel Le Gallo, and Daniel Krebs, Nature communications, 2014