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Origin of Border Traps in Normally-off Al_2O_3/GaN MOSFET with Different Gate Recess Techniques

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Abstract

Border traps in normally-off Al_2O_3/GaN MOSFET with different gate recess techniques are investigated by low frequency noise measurement and ac transconductance method. Lower drain current spectral density of 1/f form and less dispersive ac transconductance are observed in MOSFETs with oxygen assisted wet etching compared with devices with ICP dry etching. One decade lower border trap density is extracted by both methods in oxygen assisted wet etching devices compared with conventional dry etching gate recess devices. The ICP dry etching gate recess with large damage presents rough and active surface that is prone to form detrimental Ga_xO validated by atomic force microscopy and X-ray photoelectron spectroscopy. The Ga_xO located closed to the interface is the major location of border traps. The damage-free oxidation assisted wet etching gate recess technique presents relatively smooth and stable surface, which would lead to better MOS channel quality and improved device reliability.

1. Introduction

With high electron mobility, high breakdown electric field and high density two-dimensional electron gas (2DEG), the AlGaN/GaN high mobility transistor (HEMT) is widely studied as a promising candidate for high power electronic applications. For power switch applications, enhancement mode (E-Mode) GaN MOSFET utilizing gate recess combined with high quality high-*k* gate insulators deposited by atomic layer deposition (ALD), such as Al_2O_3, is more applicable due to its large gate swing and low gate leakage current. In such devices, reliable dielectric with low trapping effect is highly desired for good channel transport property and long term reliability.

The surface morphology of the GaN layer after gate recess, which is closely related to the recess method, would also greatly influence the quality of the gate insulator. It has been reported that the oxide traps in SiO_2 would apparently increase in spite of only a small change in roughness of silicon surface. However, such work is still lacking in GaN HEMT, especially in gate-recessed E-mode GaN MOSFET. In this letter, we present a systematic study of the border traps in Al_2O_3/GaN MOS structure using low frequency noise and ac transconductance measurements. It is found that the distribution and density of border traps is also related to the gate recess method and wet etching leads to a smaller density of border traps comparing with the conventional ICP dry etching process, which is supposed to originate from the reduced Ga-O bonds at the GaN surface as a result of smooth surface after recess.

2. Result and Discussions

The HEMT structure consists of a 4-μm-thick C-doped buffer layer, a 300 nm undoped GaN layer, and a 30 nm undoped $Al_{0.25}Ga_{0.75}N$ barrier layer. Device A was fabricated by an oxidation and wet etching-based gate recess process to eliminate the plasma induced damage.[1] Device B is fabricated by conventional low-power ICP dry etching.[2] The thickness of the Al_2O_3 layer in device A and B was 20 and 25 nm, respectively. Similar threshold voltage is observed in both devices but the output current density is much higher in device A owing to the reduced damage during gate recess (shown in Fig. 1(a)). The surface morphology of the GaN channel after gate recess in device A and B was measured by AFM (not shown here). Atomic step could only be observed in device A. The root mean square (RMS) roughness of the surface in device A is 0.33 nm and the one in device B is 0.59 nm. GaN surface after wet etching is much smoother since there is no high energy ion bombardment in the wet based gate recess process, which provide a mild chemical reaction environment. In order to get insight into the effects of different gate recess techniques on chemical composition of the etched surface, XPS measurement was conducted on the two samples after recess (not shown here). We found that the surface of device B is more nitrogen-deficient owing to the large plasma damage during ICP dry etching. The N-deficient surface would easily absorb oxygen and form thin Ga_xO layers on the as etched GaN surface. Besides, the thin Ga_xO layer should be defective as a result of rough surface, which would lead to trapping effect in the oxide layer. On the other hand, the Ga_xO component in device A was suppressed due to the smoother surface morphology.

The low frequency noise measurement is conducted on the MOSFET by the use of low noise current amplifier and signal analyzer, covering a frequency range from 10 Hz to 10 kHz. The drain voltage is set to 0.2 V to ensure the energy band bending along the channel can be neglected. The drain current noise is measured at different current magnitudes by varying the gate voltage. As shown in Fig. 1(b), drain current noise in devices with wet etching based gate recess process is much smaller than the one in devices with conventional ICP dry etching, suggesting increased trapping/detrapping process from the border traps in the dielectric layer grown on nitrogen-deficient surface at the same current level. As shown in Fig. 1(c) and (d), the normalized drain current noise of both devices have the same variation trend with $(g_m/I_D)^2$ as drain

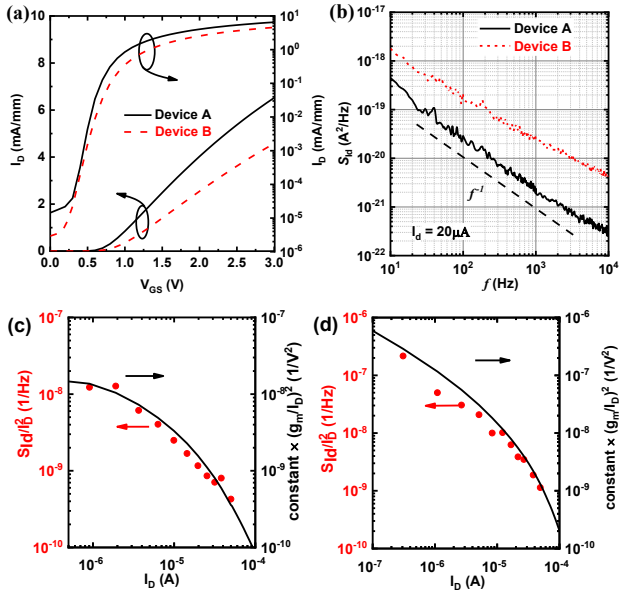

Fig. 1 (a) Transfer characteristics of device A (black) and device B (red) at V_{DS}=0.2 V, (b) Drain current noise spectral density of device A (solid-black) and device B (dash-red) at V_{DS}=0.2V, I_D=20 μA, and normalized drain current noise spectral density $(S_{Id}/I_D)^2$ and $(g_m/I_D)^2$ for (c) Device A, and (d) Device B at V_{DS}=0.2 V at f=10 Hz.

current varying several magnitudes, indicating that $1/f$ noise can be interpreted by carrier number fluctuation model due to mobile carrier capture/emission in the gate oxide as the following equation, $S_{Id}/I_d^2 = (g_m/I_d)^2 S_{Vfb}$, with $S_{Vfb} = q^2 N_t kT\lambda/WLC_{ox}^2 f^{\gamma}$, where S_{Vfb} is the power spectral density of flatband voltage fluctuation with N_t being the volume trap density, kT is the thermal energy, λ is the oxide tunneling attenuation distance given by $\lambda=[4\pi(2m^*\Phi_B)^{1/2}/h]^{-1}$ where m^* denoting the effective electron mass and Φ_B is the oxide barrier height, WL is the channel area, C_{ox} is the oxide capacitance per unit area , f is the frequency and γ is the frequency exponent. The extracted γ for device A ranges from 0.95 to 0.99 and from 0.82 to 0.85 for device B in the measurement range of the drain current. It was explained that $\gamma<1$ was attributed to nonuniform oxide trap states distribution. For a trap distribution that is skewed toward the interface, there are a larger number of traps with short time constant, which would lead to $\gamma<1$. As a result, the density of border traps located closed to the MOS interface in device B should be higher than the one in device A. We speculate that there exists much higher density of border traps in the native oxide Ga_xO based on XPS measurement. According to the carrier number fluctuation model, the extracted values of border trap density is $1.4\times10^{18} \sim 2.6\times10^{18}$ $eV^{-1}\cdot cm^{-3}$ for device A and $9.3\times10^{18} \sim 1.9\times10^{19}$ $eV^{-1}\cdot cm^{-3}$ for device B, respectively.

Ac transconductance measurement is conducted to get the spatial distribution of border traps in the MOSFET. The drain voltage is set to be 0.2 V with the current amplifier. During the measurement, a DC bias mixed with an ac sinusoidal signal (amplitude of 20 mV, frequency of f) is applied on the gate, and the ac-g_m is calculated in the frequency range of 10 Hz to 20 kHz. The frequency dispersion of the ac-g_m is attributed to the variation of carrier density in the channel caused by carrier capture/emission by the border traps. The

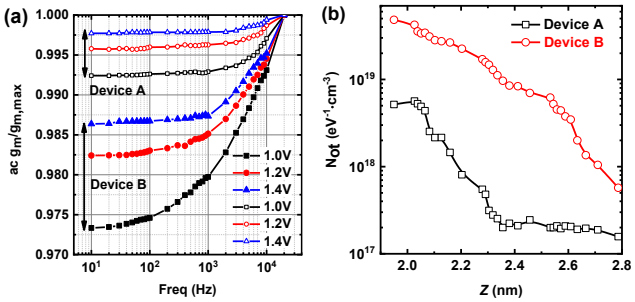

Fig. 2 (a) Normalized ac-g_m dispersion of device A and B at V_{DS}=0.2 V, and (b) the distribution of border trap in the gate dielectric of device A and B at V_{GS}=1 V.

border traps with τ larger than $1/f$ are not likely to respond to the ac signal and therefore have little influence on the g_m dispersion. Fig. 6(a) shows the normalized ac-g_m dispersion with the frequency of the ac signal. The density distribution of border traps could be extracted from the ac-g_m dispersion by $N_{ot}(x) = \frac{dg_m}{dlnf}[\frac{x}{x_0}(1-\frac{x}{x_0})q\lambda\beta]^{-1}$, where $\beta = W\mu V_{DS}/L$ can be determined from the transfer curve and C-V measurement, x_0 is the oxide thickness, the oxide trap position x can be calculated as $x=\lambda ln(1/f\tau_0)$, in which $\tau_0 \approx (n_0 v_t \sigma_n)^{-1}$. It's common for device A and B that the border trap density decreases as the location of the traps moves away from the MOS interface as shown in Fig. 2(b), suggesting that surface morphology and surface chemical component have important effect on the quality of the oxide layer. The wet based gate recess technique eliminates high energy ion bombardment damage on the GaN surface, results in smoother and near stoichiometry surface, preventing the formation of thick GaO_x layer with large density of traps.

3. Conclusions

Lower density of border traps is observed in gate oxide grown on the GaN surface exposed by oxidation assisted wet etching based gate recess method in normally-off GaN MOSFET. Rough and nitrogen-deficient surface after ICP-based gate recess is prone to be oxidized and form detrimental Ga_xO layers with high density of defects, which leads to much higher density of border trap in the MOS gate structure in the enhancement-mode GaN MOSFET with ALD grown Al_2O_3 gate insulator. The better surface morphology and lower density of border traps in devices with wet etching would lead to better transport properties of the carriers in the MOS channel and improved reliability of the gate insulator.

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