Extended Abstracts of the 2018 International Conference on Solid State Devices and Materials, Tokyo, 2018, pp967-968

Negative bias instability of β-Ga_2O_3 nanomembrane field-effect transistors

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Abstract

In this poster, we report on negative bias stress (NBS) instability of β-Ga_2O_3 nanomembrane FETs fabricated by mechanical exfoliation. Although the devices exhibit high electrical performance of field-effect mobility ~ 71.6 due to high crystal quality of β-Ga_2O_3, we observe abnormal threshold voltage shift under NBS condition. The result indicates device high quality of surface passivation is required to ensure device's performance.

1. Introduction

Recently, gallium oxide (Ga_2O_3) has attracted much attention for next generation power device applications, because of its large bandgap (E_g) and high Baliga's figure of merit (BFOM) compared to those of SiC and GaN [1]. It also shows n-type conductivity attributed to oxygen vacancies and unintentional Si incorporation with Ga_2O_3 powder. β-Ga_2O_3's monoclinic structure has relatively a large lattice constant of 12.23Å along the [100] direction, while that of in the [010] and [001] direction is 3 Å and 5.8 Å, respectively [2]. Although β-Ga_2O_3 is not a two dimensional van der Waals layered materials, this unique structure allows a facile cleavage into nanomembrane along [100] direction, and there have been several reports based on the exfoliation method [3,4]. For our best knowledge, however, this is the first report on NBS instability of β-Ga_2O_3 FETs with bottom-gate configuration using mechanically exfoliated β-Ga_2O_3 nanomembrane from its bulk crystal.

2. Device fabrication and Measurement

Heavily doped p-type Si substrate with thermally grown 300nm SiO_2 layer were cleaned in acetone and IPA (Isopropyl alcohol) for 5min. Using conventional scotch tape method, β-Ga_2O_3 nanomembrane was transferred to the substrate, which was mechanically exfoliated from unintentionally doped Bulk β-Ga2O3 crystals (Tamura corp., Japan) with a (-201) surface orientation; its effective donor carrier concentration (N_d-N_a) approximately was 4.8 x 10^{17} cm^3. The source and drain region were defined by conventional photolithography, followed by Cr/Au (20/100 nm) metallization using evaporator and then lift-off process patterned source and drain electrodes. We investigated the electrical parameters and bias instability of β-Ga_2O_3 nanomembrane field-effect transistors (FETs) using current-voltage (I-V) measurement and negative gate bias stress test at room temperature using a semiconductor parameter analyzer (HP 4145B). Channel thickness was analyzed by AFM (PSIA, XE-150).

3. Results and discussions

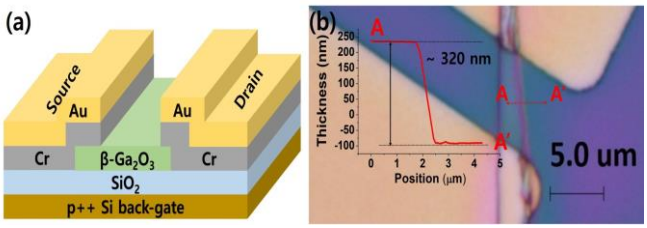

Fig. 1 (a) cross-sectional schematic of β-Ga_2O_3 nanomembrane FET, (b) optical microscope image of fabricated β-Ga_2O_3 nanomembrane FET (Inset) Thickness profile of channel layer (Device B).

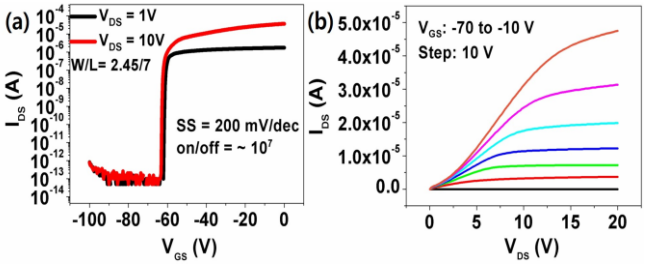

Fig. 2 (a) Transfer characteristics and (b) Output characteristics of the measured β-Ga_2O_3 nanomembrane FET (Device B).

Fig. 1(a) and (b) show cross-sectional schematic and optical microscope image of the fabricated β-Ga_2O_3 nanomembrane FET. We confirmed the thickness of β-Ga_2O_3 channel layer was ~ 320 nm using AFM as shown in the inset of Fig.1 (b). Channel width (W) and length (L) were 2.45 μm and 7 μm, respectably. The capacitance of 300nm SiO_2 was 1.15 x 10^{-8} F/cm^2.

Fig. 2(a) represents the measured transfer curve of I_{DS}-V_{GS} for V_{DS} = 1 and 10 V. At V_{DS} = 1 V, it shows on/off ratio of 10^7, field effect mobility (μ_{EF}) of 71.6 $cm^2/V{\cdot}s$ and subthreshold (SS) of 200 mV/dec, which were calculated from following eq. (1) and (2), respectably.

$$\mu_{EF} = \left(\frac{L}{W}\right) \cdot \frac{g_m}{C_{OX} \cdot V_{DS}} \qquad (1)$$

$$SS = \frac{d(V_{GS})}{d(\log_{10}(I_{DS}))} \qquad (2)$$

Low SS indicates high quality of the interface between β-Ga_2O_3 and SiO_2 was formed. Threshold voltage (V_{TH}) was about -60 V extracted from the linear extrapolation of transfer characteristics curve. Fig. 2(b) shows output curves with

good saturation and pinch-off at high V_{DS} bias; it was measured from V_{GS} = -70 to -10 V as 10 V step, sweeping from V_{DS} = 0 to 20 V. electrical parameters of the fabricated devices are summarized in Table I

Table I Summary of electrical parameters

Device	V_{TH} [V]	μ_{EF} [$cm^2/V{\cdot}s$]	SS [mV/dec]	On/off
A	-82.1	26.02	260	$4{\cdot}10^6$
B	-61.02	71.57	200	$2{\cdot}10^7$
C	-47.25	18.82	266	$7{\cdot}10^7$
D	-84.9	33.53	301	$9{\cdot}10^5$

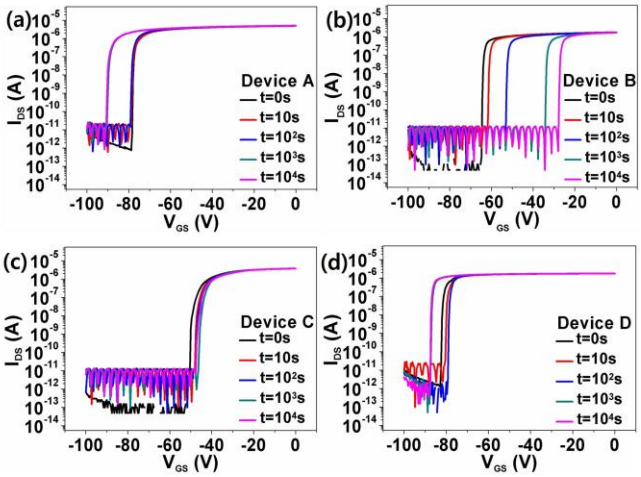

Fig. 3 NBS at device A, B, C and D (a) typically negative shift, (b) abnormally positive shift, (c) and (d) turnaround to negative direction.

To investigate electrical instability, we performed transfer characteristics measurements under NBS condition for 10,000 s at t_{stress} = 0, 10^1, 10^2, 10^3, 10^4 s. In order to set effective gate bias (= V_{GS} - $V_{TH(initial)}$) of -20 ~ -15 V, different gate bias (V_{GS}: -100 ~ -70 V) were applied.

Fig.3 shows ΔV_{TH} from the four measured devices. In general, V_{TH} tends to shift negative direction under NBS, as shown in Fig.3 (a). This is because the electrons, trapped in interface between semiconductor and SiO_2, release into channel layer. However, Fig.3 (b), (c) and (d) shows the observed abnormal ΔV_{TH} ; Device B exhibits positive V_{TH} shift from -63.9 V to -27 V (i.e. ΔV_{TH} = 36.9 V). The amount of ΔV_{TH} of C and D were 3.69 V and 3.5 V by 10^3 s and 10^2 s. Then, interestingly enough, ΔV_{TH} of C and D shows turnaround behavior forward negative direction after t_{stress} = 1,000 s and 100 s.

These unusual cases can be explained by surface depletion effects due to defects (i.e. oxygen vacancy) and absorbed traps such as water and oxygen molecules on channel surface. In the case of Device B, as illustrated in Fig. 4(a), surface electron trapping causes surface depletion, which leads to considerable V_{TH} shift depending on the channel thickness [5]; Surface trapping seems to exceed released electrons into the channel. In return, ΔV_{TH} is positive.

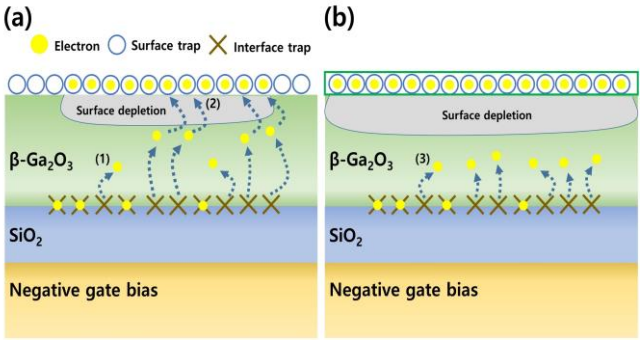

Fig. 4 Schematic of surface and interface trapping at NBS: (a) electron release into channel (1). Simultaneously, surface electron trapping occurs (2). (b) After surface trapping fully, electron release into channel only (3).

Using eq. (3), we calculated the surface trapped electron concentration (Δn) after 10,000s. The Δn of Device B was estimated to 2.65 x 10^{12} cm^{-2}. Table II summarize the surface trapped electron concentration Δn of Device B, C and D.

$$\Delta n = Q / e = C_{OX} \cdot (\Delta V_{TH}) \qquad (3)$$

Table II surface trapped electron concentration

Device	B by 10^4 s	C by 10^3 s	D by 10^2 s
Δn [cm^{-2}]	$2.65{\cdot}10^{12}$	$2.65{\cdot}10^{11}$	$2.52{\cdot}10^{11}$

As illustrated in Fig. 4(b), once the surface traps are filled with electrons, the fully trapped surface acts as passivation layer. Consequently, the additional electrons released into the channel lead to charge accumulation in the channel and ΔV_{TH} is negative from that point; Device D's ΔV_{TH} was -8.84 V from 10^2 s to 10^4 s. By using eq. (3), Accumulated electron concentration also can be calculated. Since turnaround, the value of Device D was estimated to 6.35 x 10^{11} cm^{-2}

4. Conclusions

In this study, we report on abnormal positive and turnaround threshold voltage shift of the β-Ga_2O_3 FET under negative bias stress. It results from the surface depletion effects due to surface states and absorbed oxygen and water molecules. This result suggests a high quality of passivation treatment is needed to acquire high electrical performance and stability of the β-Ga_2O_3 FET.

References

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