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Gate-All-Around $In_{0.53}Ga_{0.47}As$ MOSFETs with I_{on}=3.3mA/µm (V_{gs}-V_{th}=V_{ds}=1V) and g_m=3.56 mS/µm (V_{ds}=0.5V) using Plasma-Enhanced Atomic Layer Deposition Technique

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Abstract

In this article, $In_{0.53}Ga_{0.47}As$ GAA FETs are fabricated using the advanced interfacial passivation treatments achieved by plasma-enhanced atomic layer deposition (PEALD) technique. Device with L_{ch} = 50 nm exhibits $I_{on}/I_{off} > 10^4$, *SS* = 105 mV/dec at V_{ds} = 0.5 V, DIBL = 100 mV/V, I_{on} = 3.3 mA/µm at $V_{gs} - V_{th} = V_{ds}$ = 1 V. We show an I_{on} per fin of 0.213 mA/µm at $V_{gs} = V_{ds}$ = 0.5 V and a $g_{m,\ max}$ = 3.56 mS/µm at V_{ds} = 0.5 V, which are among highest values reported for III-V FETs of any kind including MOSFETs and HEMTs. These results are attributed to the superior high-k/III-V quality enabled by PEALD treatments, boosting the performances of III-V FETs in future CMOS logic applications.

1. Introduction

Among III-V compound semiconductors, $In_xGa_{1-x}As$ materials have been widely investigated as promising n-channel candidates to replace Si in next generation high-performance and low-power electronic applications [1]. To continue CMOS technology scaling, FinFETs and gate-all-around (GAA) FETs are proposed as fully-depleted structures that provide strong electrostatic control of the transistor channels. In spite of many progresses to realize InGaAs-based FinFETs or GAA FETs with superior performances [2] – [8], several key challenges remain to be improved. One of those is the etching-induced-damage at the channel sidewall along with the nature poor quality of high-k/III-V interfaces, requiring advanced MOS interfacial engineering. In this work, we fabricate $In_{0.53}Ga_{0.47}As$ GAA FET applying the plasma-enhanced atomic layer deposition technique (PEALD) as pre- and post-gate passivation treatments. We demonstrate high performance InGaAs GAA FET with a drive current, I_{on}, of 3.3 mA/µm at $V_{gs} - V_{th} = V_{ds}$ = 1 V, and a transconductance, $g_{m,\ max}$, of 3.56 mS/µm at V_{ds} = 0.5 V. This $g_{m,\ max}$ is a record value among III-V FETs of any kind including MOSFETs and HEMTs.

2. Experimental Procedure

The InGaAs GAA FETs were fabricated using a top-down gate-last process following that of our previous work [6]. Epitaxial structures used in this study consisted of 50 nm p-$In_{0.53}Ga_{0.47}As$ (5×10^{16} Be doped) channel layer and 100 nm p^+-InP buffer layer on a p^{++}-InP substrate grown by solid source molecular beam method. A 10-nm Al_2O_3 was grown by atomic layer deposition (ALD) as a dummy layer. Source/drain Si implantation was then performed and activated by the rapid thermal annealing. Then, the fin was defined via electron-beam lithography. The fin profile was done by inductively coupled plasma (ICP) dry etching and citric acid wet etching. After chemical treatment with HCl and $(NH_4)_2S$, samples were loaded into ALD chamber for PEALD processes. The AlN interfacial passivation layer (~ 1 nm), HfO_2 gate oxide (5 nm) and post-remote-plasma treatment in nitrogen were applied as described elsewhere [9] – [11]. Post deposition annealing was applied at 450 °C in forming gas ambient. TiN gate metal, Au/Ge/Ni/Au S/D ohmic, and AuB backside contact were formed and finished by post metallization annealing. Fig. 1 shows the cross-sectional TEM images of (a) a completed GAA structure and (b) a nanowire profile.

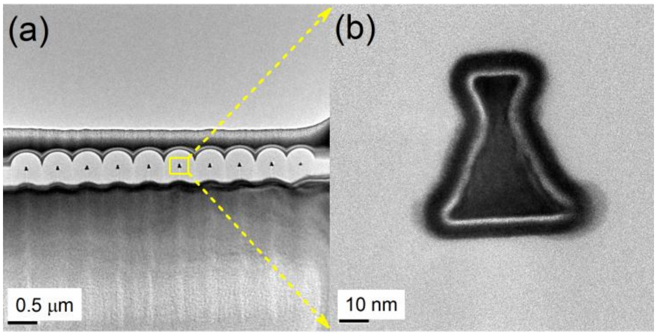

Fig. 1 Cross-sectional TEM images of (a) a completed GAA structure and (b) a nanowire profile. The final InGaAs GAA FETs were fabricated featuring 10 nanowire channels.

3. Results and Discussion

Electrical data is normalized to the total gated periphery as shown in Fig. 1 (b). Figs. 2(a) and (b) show the ouput ($I_{ds} - V_{ds}$) and transfer ($I_{ds} - V_{gs}$) characteristics of L_{ch} = 50 nm

$HfO_2/AlN/In_{0.53}Ga_{0.47}As$ GAA FET. Subthreshold swing (SS) of 98 and 105 mV/dec at V_{ds} of 0.05 and 0.5 V, respectively, and drain induced barrier lowering ($DIBL$) of 100 mV/V are observed. This device has I_{on}/I_{off} ratio of 2.23 × 10^4 at V_{ds} = 0.5 V, I_{on} of 3.3 mA/μm at $V_{gs} - V_{th} = V_{ds}$ = 1 V, and the on-resistance, R_{on}, of 265 Ω × μm at $V_{gs} - V_{th}$ = 1 V. The transconductance ($g_m - V_{gs}$) and linear $I_{ds} - V_{gs}$ characteristics are shown in Fig. 2(c). The $g_{m,\,max}$ of 3.56 mS/μm, $Q = g_{m,\,max}/SS$ = 34 at V_{ds} = 0.5 V and I_{on} of 1.52 mA/μm at $V_{gs} = V_{ds}$ = 0.5 V are obtained. Benefiting from the PEALD treatments, the performance improvements of InGaAs GAA FET are attributed to the high quality of high-k/III-V MOS interface as well as sufficient EOT scaling.

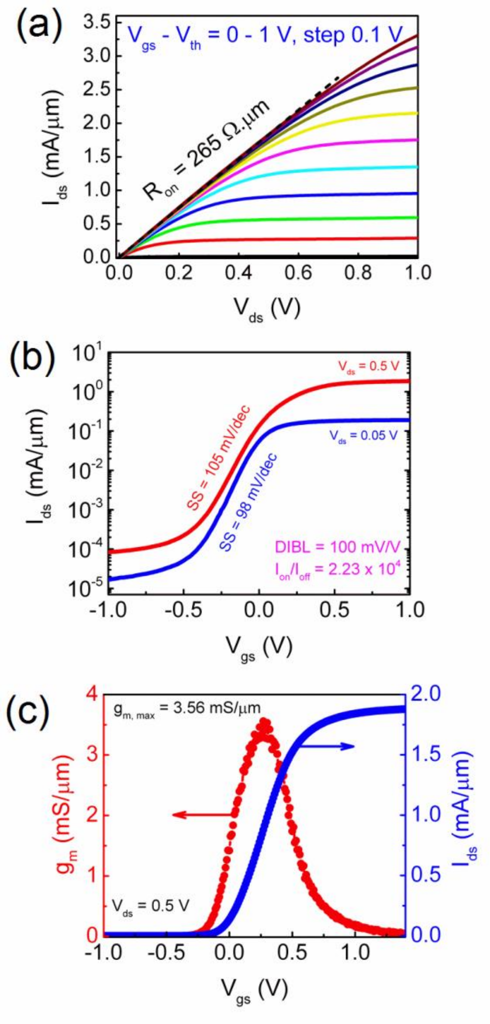

Fig. 2 (a) Output ($I_{ds} - V_{ds}$), (b) transfer ($I_{ds} - V_{gs}$), (c) transconductance ($g_m - V_{gs}$) and linear ($I_{ds} - V_{gs}$) characteristics for a L_{ch} = 50 nm $HfO_2/AlN/In_{0.53}Ga_{0.47}As$ GAA FETs fabricated with PEALD pre- and post-gate treatments.

Fig. 3(a) compares the I_{on} per fin versus L_{ch} (at $V_{ds} = V_{gs}$ = 0.5 V) achieved in this work with other reported $In_{0.53}Ga_{0.47}As$ FinFETs and GAA FETs [2] – [6]. The I_{on} of 0.213 mA/fin in our $In_{0.53}Ga_{0.47}As$ GAA FET is among the highest values reported for both categories of $In_{0.53}Ga_{0.47}As$ FETs. Fig. 3(b) benchmarks the $g_{m,\,max}$ (at V_{ds} = 0.5 V) for the state-of-the-art III-V FETs. The value of 3.56 mS/μm obtained here is the record value for III-V FETs of any kind.

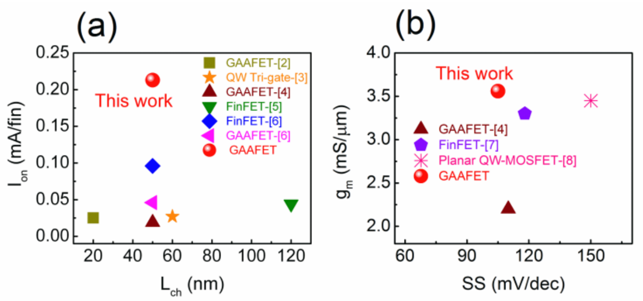

Fig. 3 Benchmark plots of (a) I_{on} per fin, at $V_{ds} = V_{gs}$ = 0.5 V, versus L_{ch} and (b) $g_{m,\,max}$, at V_{ds} = 0.5 V, versus SS. The data are compared to other reported III-V based FET devices.

4. Conclusions

We demonstrate the beneficial effects of advanced MOS interfacial technique using PEALD treatments on the electrical performance of $In_{0.53}Ga_{0.47}As$ GAA FETs. The device exhibits $I_{on}/I_{off} > 10^4$, I_{on} = 3.3 mA/μm (at $V_{gs} - V_{th} = V_{ds}$ = 1 V), I_{on} per fin of 0.213 mA/fin (at $V_{gs} = V_{ds}$ = 0.5 V), SS = 105 mV/dec, the record $g_{m,max}$ = 3.56 mS/μm, and $Q = G_m/SS$ = 34 at V_{ds} = 0.5 V. These results are attributed to the superior high-k/III-V interface quality achieved by the PEALD treatments. This is pushing the potential of III-V based MOSFETs toward its limitation for next-generations of CMOS technology.

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References

[1] J. A. del Alamo, Nature. 479(2011) 317.
[2] J. J. Gu *et al., IEDM Tech. Dig.* (2012) 634.
[3] T. D. Kim *et al., IEDM Tech. Dig.* (2013) 425.
[4] N. Waldron *et al., IEDM Tech. Dig.* (2015) 799.
[5] M. L. Huang *et al.*, *VLSI Technology and Circuits* (2016) 1.
[6] Q. H. Luc et al., IEEE Electron Device Lett. 39 (2018) 339.
[7] C. B. Zota et al., IEDM Tech. Dig. (2015) 811.
[8] J. Lin et al., IEEE Electron Device Lett. 37 (2016) 381.
[9] Q. H. Luc et al., IEEE Electron Device Lett. 36 (2015) 1277.
[10] Q. H. Luc et al., IEEE Electron Device Lett. 37 (2016) 974.