

Evaluations of Minority Carrier Lifetime in FZ-Si Affected by Si-IGBT Processes

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Abstract

This study evaluated minority carrier lifetime in FZ-Si affected by Si-IGBT processes. Silicon gate-oxidations deteriorated lifetime due to the formation of the interface states between silicon and oxide. Therefore, the cross-sectional photo-luminescence imaging shows that the lifetime around trench is lower than that of the bulk region. The high temperature thermal treatment for the B-base/P-emitter layer activation after gate-oxidation improved the interface, thus resulted in the recovery of the lifetime.

1. Introduction

Si insulated gate bipolar transistors (IGBTs) are attractive for the implementation to large commodity markets [1]. Performance improvements in the trench-gate Si-based IGBT have been developed on the base of 3D scaling that enhances carrier injection [2]. In addition to the 3D scaling, the minority carrier lifetime control is an important issue [3], for further performance improvement.

For this purpose, we have evaluated minority carrier lifetime in FZ (Floating Zone)-Si affected by the IGBT processes, especially gate oxidation, poly-Si deposition and the following thermal treatment for the B-base/P-emitter layer activation. The evaluations were performed using the photoconductive decay method [4], cross-sectional and conventional plan photo-luminescence (PL) imaging [5].

2. Experiment

Samples were fabricated using 3-inch n-type (001) FZ-silicon substrates. The trench-gate structure, whose width and depth of 3 and 6 μm , were fabricated by a conventional lithography and dry etching process along $\langle 110 \rangle$ direction. The substrates with and without trench gate structure after appropriate cleaning including a sacrificial oxidation for the trench structures were oxidized by the wet (900°C, 12min, H₂O ambient) or dry (1050°C, 16min, O₂ ambient) conditions. Then p-doped poly-Si was deposited to fill the gate electrode for some of the trench samples. The samples without trench-gate were thermally treated at 1050°C for 60min in an N₂ ambient to simulate the activation process for the B-base/P-emitter layers.

Lifetime was measured by the photoconductivity decay method using Sinton CT-120 [4]. The lifetime measurements were performed for the silicon with oxide films formed by dry/wet oxidations, and for the silicon with surface passivation by quinhydrone methanol [6] after removing the

oxide film.

Cross-sectional PL imaging was carried out for the sample with trench-gate. The excitation wavelength of 808 nm, whose penetration depth into Si is approximately 10 μm , was used so that the surface damage due to the cross-section preparation processes did not affect significantly. The filter in front of the InGaAs imager was band pass filter (1140 \pm 90 nm) to observe band edge PL emission. It is well-known that the band edge PL intensity is proportional to the lifetime [7]. The cross-sectional sample was formed by Ar⁺ ion etching with metal mask.

For the PL imaging from the surface through the oxide film was performed with the UV(355 nm) excitation which is transparent for SiO₂ and quinhydrone passivation with the penetration depth into Si of approximately 10 nm. Thus, we can evaluate the lifetime close to the interface. The same band pass filter and InGaAs imager as for cross-sectional PL imaging were also used for the evaluation.

3. Results and Discussion

The lifetime measurement results for the samples with oxide film formed by dry/wet oxidations and for those with quinhydrone methanol passivation after removing the oxide films are shown in Fig.1. This figure shows that (1) the lifetimes for quinhydrone methanol passivation after oxide film removal are higher than those with oxide films, and that (2) the lifetime is higher in the order of “dry oxide without trench” > “dry oxide with trench” > “wet oxide without trench” > “wet oxide with trench”.

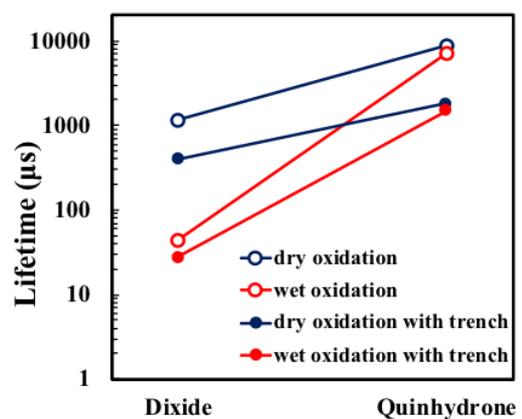


Fig. 1 Lifetime after oxidation by dry/wet conditions and with quinhydrone methanol passivation after removing the oxide films

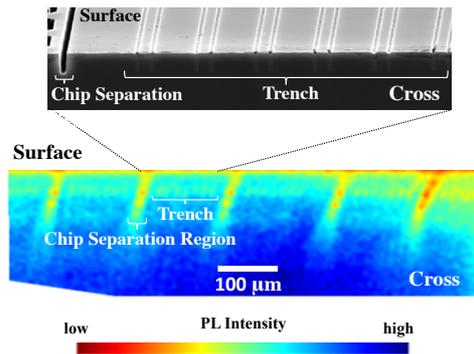


Fig. 2 Cross sectional PL imaging for the trench structure after poly-Si deposition and SEM image

The result (1) indicates that lifetime degradation after gate oxidation is not caused by bulk defects, but by the interface states between silicon and oxide film. It is also confirmed the density of interface states with wet oxide film is larger than that with dry oxide film which is verified by the C-V measurements. The result (2) shows that the lifetime decreased by the trench fabrication, which can be explained by the increase of the interface area and the (110) interface contribution.

The cross sectional PL image for the trench structure with poly-Si gate electrode after dry oxidation and the SEM image are shown Fig. 2. As shown in Fig. 2, the PL intensity around the trench is lower than that of bulk region. It means that the lifetime around trench is lower than that of the bulk region.

The PL images from the surface before and after thermal treatment for the samples with oxide film formed by dry and wet oxidations are shown in Figs. 3 and 4, respectively. These figures show that PL intensities after thermal treatment are higher than those before the annealing. This may reflect the decrease in the interface states by the thermal treatment for the P/B activation simulation.

4. Conclusions

We have evaluated minority carrier lifetime in FZ-Si affected by the IGBT processes, especially gate oxidation, poly-Si deposition and the following thermal treatment for the base/emitter activation. Conclusions are as follows.

- 1: Silicon gate-oxidations form interface states between silicon and oxide, where the states density by the wet oxidation is larger than the dry oxidation. This interface states causes in the lifetime degradation in FZ-Si.
- 2: A cross-sectional photo-luminescence imaging shows that the lifetime around trench is lower than that of the bulk region.
- 3: The high temperature thermal treatment for the B-base/P-emitter activation after gate-oxidations improves the interface between silicon and oxide.

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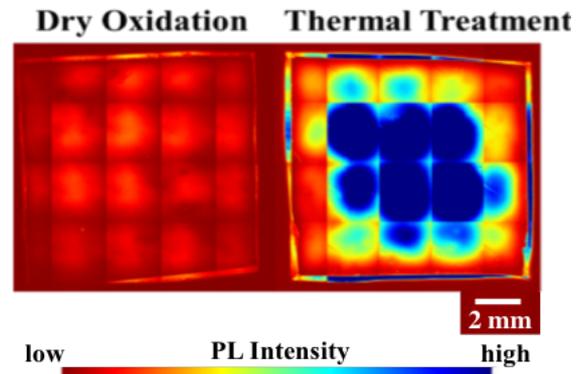


Fig. 3 PL images before and after thermal treatment with dry oxidized film.

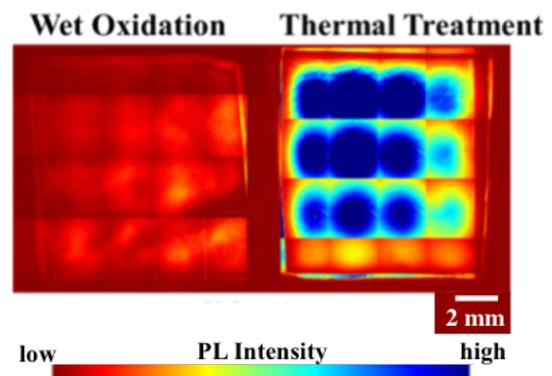


Fig. 4 PL images before and after thermal treatment with wet oxidized film.

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References

- [1] B. J. Baliga, IEEE Electron Dev. Lett., 4, 452 (1983).
- [2] K. Kakushima, *et al.*, Tech. Dig. of IEDM, 268 (2016).
- [3] N. Iwamoto *et al.*, IEEE Trans. Electron Device, **64**, 741 (2017).
- [4] D. E. Kane and R. M. Swanson, IEEE PVSC, 578 (1985).
- [5] G. Kato, *et al.*, Jpn. J. Appl. Phys. Lett. 90, 093560 (2007).
- [6] B. Chhabra, Appl. Phys. **96** 063502 (2010).
- [7] J. Haunschild, *et al.*, Sol. Energy Mater. Sol. Cells, 10,1016 (2010)