Extended Abstracts of the 2018 International Conference on Solid State Devices and Materials, Tokyo, 2018, pp987-988

InGaAs Negative Capacitance FETs Using $HfZrO_x$: Impact of Annealing Conditions on the Ferroelectric and Steep Subthreshold Slope Characteristics

Quang-Ho Luc[1,2], Kai Yun Zhang[3], Yu Da Jin[4], Sa Hoang Huynh[1], Minh Thien Huu Ha[1], Huy Binh Do[1], Ping Huang[2], Che-Wei Hsu[1], Yueh-Chin Lin[1], and Edward Yi Chang[1,2,3*]

[1] Department of Materials Science and Engineering
[2] International College of Semiconductor Technology
[3] Department of Electronics Engineering
[4] Institute of Lighting and Energy Photonics
National Chiao Tung Univ.
1001 University Road, Hsinchu 300, Taiwan
Phone: +886-3-5131502; E-mail: edc@mail.nctu.edu.tw

Abstract

In this article, we demonstrate the impact of annealing conditions on the ferroelectric (FE) and steep subthreshold slope (*SS*) properties of InGaAs negative capacitance (NC) MOSFETs using $HfZrO_2$ (HZO) thin film as a gate dielectric. After annealing activation, the steep switching behaviors are achieved, attributing to the NC effect. The FE-HZO $In_{0.53}Ga_{0.47}As$ NC MOSFET device exhibits counter-clockwise I_{ds}-V_{gs} hysteresis as well as minimal *SS* of 30 and 11 mV/dec for forward and reverse bias sweeps, respectively.

1. Introduction

Steep subthreshold slope (*SS*) transistors have attracted the great interest in order to satisfy the quest of future ultra-low-power applications. Negative capacitance field-effect transistor (NCFET) is emerged as one of the promising steep *SS* transistors to suppress the supply voltage and minimize the leakage current [1]. $Hf_{0.5}Zr_{0.5}O_2$ (HZO), owing to its ferroelectric (FE) properties, is currently being investigated as a gate dielectric for realizing NCFETs. Sub-60 mV/decade *SS* has been presented in Si, Ge, and GeSn NCFETs using HZO thin film [2]-[4]. Steep switching has not been reported in InGaAs materials that are proposed as alternative channels to replace Si in next generations of CMOS technology. Here, we have applied HZO/Al_2O_3 in InGaAs channel using a gate last process to fabricate NC MOSFETs. The influences of annealing conditions on the FE as well as steep *SS* properties of InGaAs MOS devices using HZO material system are demonstrated.

2. Experimental Procedure

The epitaxial structure used in this study consisted of 50 nm p-$In_{0.53}Ga_{0.47}As$ (5×10^{16} Be doped) channel layer and 100 nm p^+-InP buffer layer on the p^{++}-InP substrate grown by solid source molecular beam method. The gate last scheme was used to fabricate the $In_{0.53}Ga_{0.47}As$ NC MOSFETs as described in Fig. 1. After surface degrease, a 10-nm Al_2O_3 was grown by atomic layer deposition (ALD) as a dummy layer. Source/drain (S/D) Si implantation was then performed and the dopant activation was carried out by rapid thermal annealing in a nitrogen ambient. The ALD deposition temperature was 250 °C. After chemical pre-gate treatment with HCl and $(NH_4)_2S$, 10-half-cycle TMA pretreatment [5] and an Al_2O_3 interfacial passivation layer were performed in ALD chamber to improve the quality of InGaAs MOS interfaces followed by an 8-nm HZO thin film. Post deposition annealing (PDA) was performed at 500 °C for 5 minutes in forming gas [6]. After TiN gate metal formation, the crystallization of HZO was activated by different post metallization annealing (PMA) conditions. Finally, S/D ohmic and backside contacts were formed. The control sample was fabricated without PMA condition for comparison. The FE properties of HZO films were evaluated by MOS capacitors (MOSCAPs) fabricated using identical PMA conditions on the same InGaAs wafer.

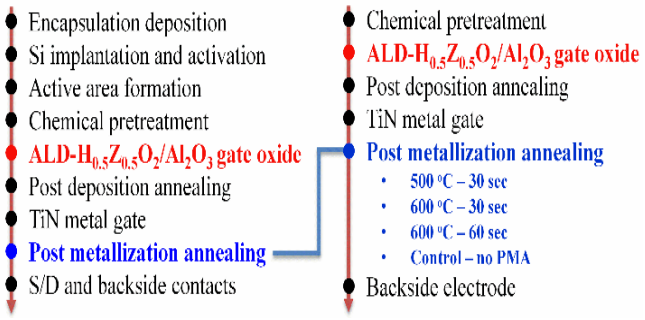

Fig. 1 Gate-last process flow for the InGaAs NC MOSFETs and MOSCAPs using HZO/Al_2O_3 gate stack.

3. Results and Discussion

Fig. 2 shows the FE nature of HZO thin film evaluating by the (a) - (b) the polarization (*P-V*), (c) displacement current (*I-V*), and (d) capacitance (*C-V*) characteristics. The expected polarization switching behaviors are seen for all samples (Fig. 2(a)). The remnant polarization (2Pr) of sample underwent PMA at 600 °C for 60 sec increases more than 4 times as compared to the control – no PMA – one (Fig. 2(b)). This proves that the PMA process provide a great effect on the HZO's crystallization and FE properties. In Fig. 2(c) and (d), the typical butterfly shaped hysteresis loops can be clearly observed in the *I-V* and *C-V* results, validating the strong FE characteristics of the PMA samples [2]. Fig. 3 compares the transfer and *SS* characteristics (I_{ds}-V_{gs}) between the MOSFET

samples with and without PMA process. All devices have a gate length of 6 µm and a gate width of 100 µm. Obviously, the steep *SS* behaviors are consistent with the FE properties after PMA activation. The NC effect enables steeper switching and lower leakage current in PMA samples as compared to the control counterpart (Fig. 3(a)). The *SS* versus I_{ds} for the fabricated InGaAs MOSFETs is presented in Fig. 3 (b). Sub-60 mV/dec *SS* is seen over two decades of drive current. For higher PMA temperature and longer duration, slight degradation in sub-60 mV/dec *SS* can be attributed to either the dielectric leakage or MOS interface quality issues.

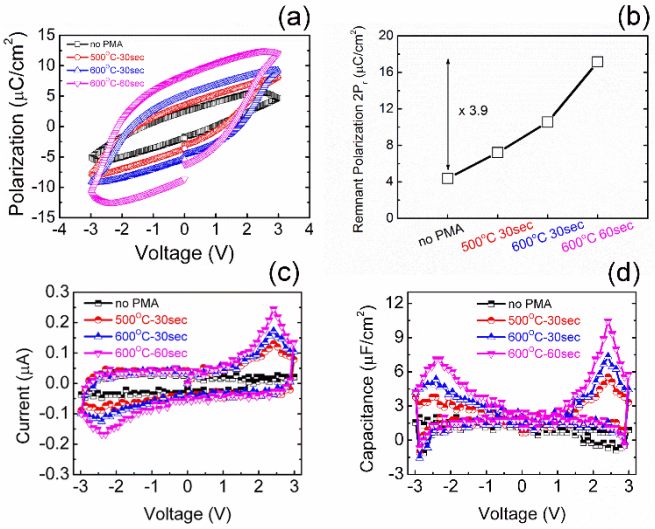

Fig. 2 (a) and (b) Polarization (*P-V*), (c) displacement current (*I-V*), and (d) capacitance (*C-V*) against bias voltage characteristics.

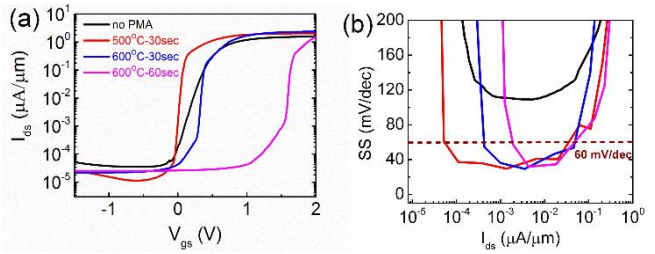

Fig. 3 (a) Transfer and (b) *SS* characteristics against V_{gs} at V_{ds} of 0.05 V for the InGaAs MOSFETs with and without PMA. The sub-60 mV/dec *SS* property can be observed only for PMA-treated HZO/Al_2O_3/InGaAs NC MOSFETs.

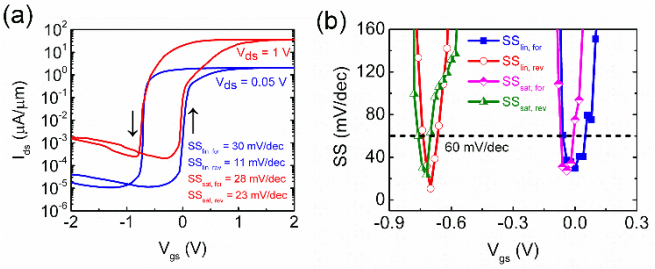

Fig. 4 (a) Transfer and (b) *SS* characteristics of the InGaAs NC MOSFET obtained by the optimized PMA condition. This device shows the minimum *SS* of 11 and 23 mV/dec at V_{ds} of 0.05 and 1 V, respectively, as well as I_{ds}-V_{gs} hysteresis of ~ 0.67 V. This can be further improved by adjusting the activation conditions and thickness of FE HZO materials system.

Fig. 4 presents the transfer and *SS* characteristics of the InGaAs NC MOSFET obtained by the optimized PMA condition. This device exhibits the minimum *SS* of 11 and 23 mV/dec at V_{ds} of 0.05 and 1 V, respectively. The trend of strong NC effect occurring in the reverse bias sweep is in accordance with literature reports on HZO-based NCFETs [3], [4]. Fig. 5 benchmarks device parameters with the state-of-the-art reports which demonstrate steep *SS* negative capacitance FETs [2]-[4].

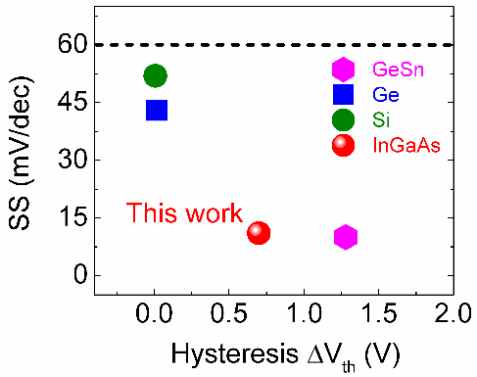

Fig. 5 Steep *SS* characteristics achieved in this work benchmark with the state-of-the-art NCFETs.

4. Conclusions

In summary, we have investigated impact of annealing conditions on the FE and steep *SS* characteristics of InGaAs NCFETs using HZO gate dielectric. The minimal forward/reverse *SS* of 30 and 11 mV/dec are obtained. Steep *SS* characteristics due to the NC effect in $In_{0.53}Ga_{0.47}As$ MOSFETs achieved in this work is very promising for future ultra-low-power III-V based CMOS applications.

Acknowledgements

This work was financially supported by the "Center for Semiconductor Technology Research" from The Featured Areas Research Center Program within the framework of the Higher Education Sprout Project by the Ministry of Education (MOE) in Taiwan. Also supported in part by the Ministry of Science and Technology, Taiwan, under Grant MOST-107-3017-F-009-002.

References

[1] S. Salahuddin *et al.,* Nano Lett. 8 (2008) 405.
[2] M. H. Lee *et al., International Electron Devices Meeting* (2015) 616.
[3] J. Zhou *et al., International Electron Devices Meeting* (2016) 310.
[4] J. Zhou *et al., International Electron Devices Meeting* (2017) 1157.
[5] Q. H. Luc *et al.,* ECS Solid State Lett. 3 (2014) N27.
[6] Q. H. Luc *et al.*, Jpn. J. Appl. Phys. 53 (2014) 04EF04.