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Scaling of Top-Gate/Bottom-Contact Pentacene-Based OFET with Amorphous Rubrene Gate Insulator

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Abstract

We have investigated the scaling of pentacene-based OFET (PB-OFET) with amorphous rubrene (α-rubrene) gate insulator utilizing lift-off process. The fabrication yield of 100% was achieved by using the Au-7.4%Ge source and drain electrodes. The top-gate (TG)/bottom-contact (BC) PB-OFET with channel length of 2.3 μm was successfully fabricated. The mobility of 5.1x10^{-3} cm^2/(Vs) was realized under the operation voltage of -5 V.

1. Introduction

The top-gate (TG)/bottom-contact (BC) type organic field-effect transistors (OFET) is necessary to be realized for future device scaling and integration. TG/BC-OFETs with polymer gate insulators such as CYTOP and PMMS have been reported [1, 2]. However, the physical thickness of the gate insulators is relatively thick such as 500 nm-1 μm. This is because the spin-coating process was used for gate insulator formation which led to the high operation voltage.

Rubrene is well known as a low-molecular organic semiconductor with high hole mobility [3]. We have reported that the fabrication of single-crystal channel OFET using rubrene narrow-line crystallization by the annealing at 170-180°C [4]. It was found that the amorphous rubrene (α-rubrene) thin film showed high thermal stability with high resistivity up to 150°C, and we have reported the fabrication of 10-20 μm channel length TG/BC pentacene-based OFET (PB-OFET) utilizing 50 nm-thick α-rubrene gate insulator [5].

In this paper, we have investigated the further scaling of the channel length down to 2.3 μm of TG/BC PB-OFET with α-rubrene gate insulator for low-voltage operation.

2. Experimental Procedure

Figure 1 shows the device fabrication process used in this study [5]. After the 10 nm-thick SiO_2 film was formed on the heavily doped n$^+$-Si(100) substrate, Au-7.4%Ge source and drain (S/D) electrodes were formed by the lift-off process using OFPR resist. Then, the surface cleaning using SPM (H_2SO_4:H_2O_2= 4:1) was carried out followed by the post metallization annealing (PMA, 115°C/2 min). Next, a 20 nm-thick pentacene (>99.995%, Aldrich) film and 65 nm-thick α-rubrene (99.99%, Aldrich) film were in-situ deposited at room temperature (RT) by thermal evaporation. Finally, an Al top-gate electrode was patterned by the lift-off process using AZ CTP-100T resist. The gate length (L) and width (W) were 2.3 - 20 μm and 30 μm, respectively.

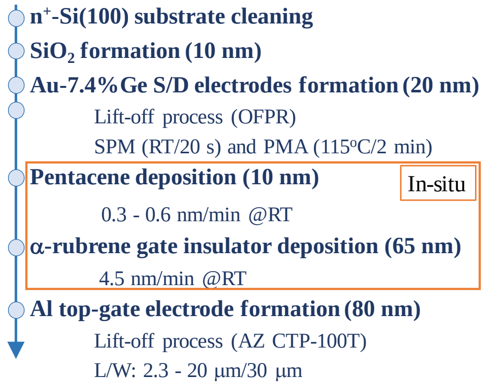

Fig. 1. Fabrication process of TG/BC PB-OFET utilizing lift-off processes.

3. Results and Discussion

Figure 2 shows the top-views and schematic cross-section of the fabricated TG/BC PB-OFETs with α-rubrene gate insulator. The Au-7.4%Ge S/D improved the fabrication yield upto 100% (Fig. 2(b)) while it was less than 5% in case of the Au S/D (Fig. 2(a)) [5]. This is because the superior adhesion properties of Au-7.4%Ge to SiO_2 improved the yield of the 2nd lift-off process for Al gate patterning. We successfully fabricated the TG/BC PB-OFETs with L of 2.3 μm utilizing Au-7.4%Ge S/D as shown in Fig. 2(c).

The extracted relative dielectric constant and equivalent

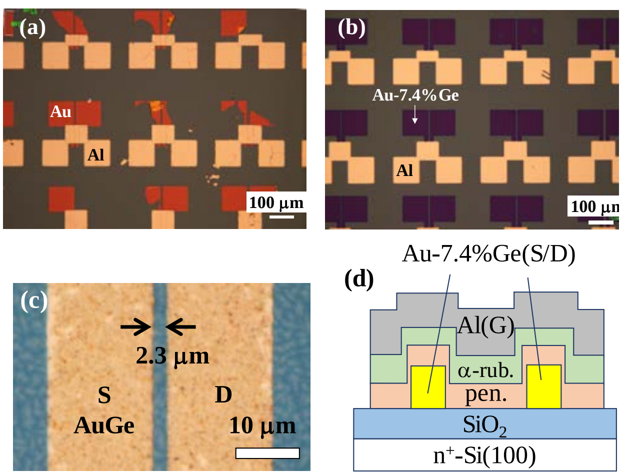

Fig. 2. Plane-views of TG/BC PB-OFETs with (a) Au S/D, (b) Au-7.4%Ge S/D, and (c) 2.3 μm channel length of TG/BC PB-OFET with Au-7.4%Ge S/D. (d) Schematic cross-section of TG/BC PB-OFET.

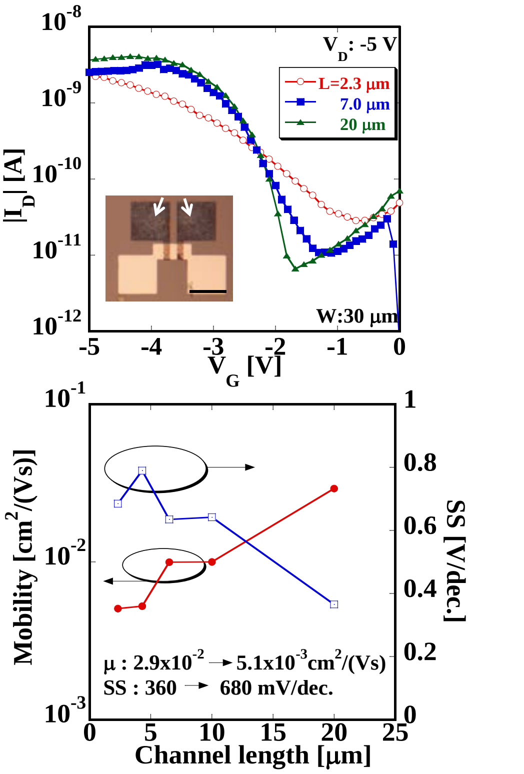

Fig. 3. Channel length dependence of (a) I_D-V_G characteristics and (b) extracted mobility and SS. L/W=2.3 - 20 μm/30 μm.

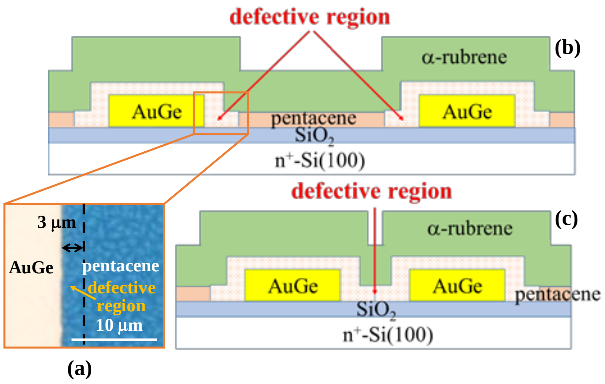

Fig. 4. (a) Surface morphology of the pentacene film at the Au-7.4%Ge S/D boundary region. The schematic cross-section describes the defective region at the S/D boundaries for (b) long channel, and (c) short channel OFET.

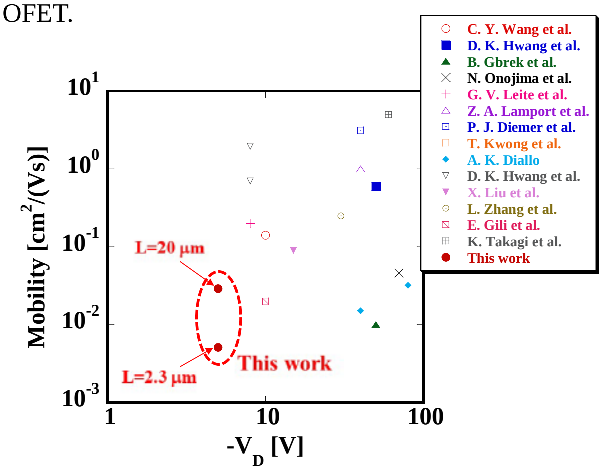

Fig. 5. Comparison of the mobility dependence on the supply voltage ($-V_D$) for the reported TG/BC-OFETs.

oxide thickness for α-rubrene gate insulator from the gate C-V characteristics (not shown) were 2.9 and 87.4 nm, respectively. Figure 3 shows the I_D-V_G characteristics and L dependence of extracted mobility and subthreshold swing (SS) for the devices with L/W=2.3 - 20 μm/30 μm. The TG/BC PB-OFET with L=2.3 μm was found to work under the operation voltage of V_D = -5 V (Fig. 3(a)), although the mobility was decreased from 2.9×10^{-2} $cm^2/(Vs)$ to 5.1×10^{-3} $cm^2/(Vs)$ and the SS was increased from 360 mV/dec. to 680 mV/dec. compared to the OFET with L=20 μm (Fig. 3(b)). The extracted density of interface states from the SS was also increased from 4.6×10^{11} $eV^{-1}cm^{-2}$ to 1.8×10^{12} $eV^{-1}cm^{-2}$ with the reduction of L from 20 μm to 2.3 μm.

Figure 4 shows the surface morphology and schematic cross-sections of pentacene film at the Au-7.4%Ge S/D boundary region of the OEFT with L=20 μm. We found that the defective regions which have a poor crystallinity with smaller grains was formed approximately 3 μm width each at the Au-7.4%Ge S/D boundaries described as shown in Fig. 4(a) [6]. The influence of defective region would also explain the abrupt decrease of the mobility and the increase of SS from the L=7 μm to 5 μm. This is because at least more than 1 μm length of ideal pentacene channel region is formed for the OFET with L=7 μm or longer as shown in Fig. 4(b). On the other hand, entire channel region turned to the defective region for the OFET with L=5 μm or shorter as shown in Fig. 4(c). The comparison of the mobility dependence on the supplied voltage ($-V_D$) for the reported TG/BC-OFETs is shown in Fig. 6. Although the mobility is not high enough, the lowest operation voltage was achieved for the TG/BC PB-OFET with α-rubrene gate insulator.

3. Conclusions

We have investigated the scaling of TG/BC PB-OFET with α-rubrene gate insulator. It was realized that the TG/BC PB-OFET with L=2.3 μm under the operation voltage of -5 V, and the extracted mobility was 5.1×10^{-3} $cm^2/(Vs)$. It is important to suppress the defective region formation to increase the mobility of the scaled TG/BC PB-OFET with α-rubrene gate insulator.

Acknowledgements

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