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Scalable Pentacene-based Pseudo-CMOS Inverter Realized by Threshold Voltage Control utilizing Nitrogen-doped LaB_6 Interfacial Layer

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Abstract

In this paper, pentacene-based enhancement/depletion-type pseudo-CMOS inverter was investigated with threshold voltage (V_{TH}) control utilizing Nitrogen-doped (N-doped) LaB_6 interfacial layer (IL) for the first time. It showed the inverter characteristics with logic swing of 1.8 V for operation voltage at -5 V. In addition, the common-gate geometry was realized for the fabricated pseudo-CMOS inverter, and it is suitable for the scaling of organic CMOS inverter.

1. Introduction

Organic field-effect transistors (OFETs) have attracted much attention because of their unique properties such as flexible and light weight, although the mobility is worse compared to that of Si. Pentacene is well known as p-type organic semiconductor, and a high hole mobility such as 1 $cm^2/(V{\cdot}s)$ was reported [1]. We have investigated pentacene-based CMOS inverter utilizing nitrogen-doped (N-doped) LaB_6 interfacial layer (IL) which has a low work function of 2.4 eV and oxidation immunity [2, 3]. We have demonstrated negative shift of threshold voltage (V_{TH}) and steep subthreshold swing of p-type pentacene-based OFETs by introducing N-doped LaB_6 IL [4]. In this paper, we proposed pentacene-based pseudo-CMOS inverter with common-gate geometry utilizing N-doped LaB_6 IL for the drive OFET. As shown in Fig. 1, pentacene-based enhancement/depletion-type pseudo-CMOS inverter with common-gate geometry would be realized due to V_{TH} control of the drive OFET to negative direction by N-doped LaB_6 IL.

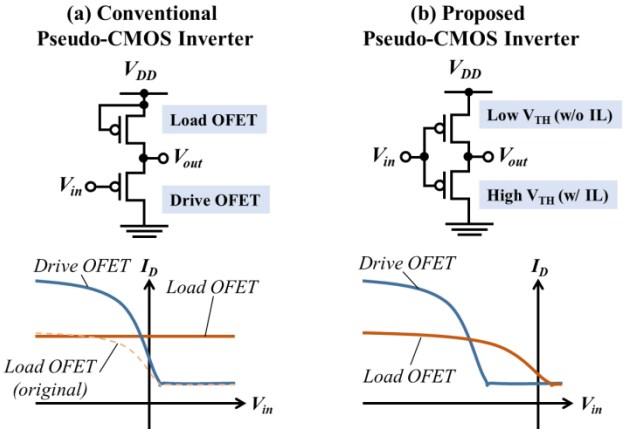

Fig. 1 Equivalent circuit diagrams and ideal I_D-V_{in} characteristics for each OFET of (a) conventional and (b) proposed pseudo-CMOS inverter in this study.

2. Experimental Procedure

The fabricated pentacene-based pseudo-CMOS inverter consisted of the back-gate/top-contact pentacene-based OFETs, as shown in Figs. 2 and 3. Heavily doped n^+-Si(100) substrate was cleaned by SPM (H_2SO_4:H_2O_2 = 4:1) and DHF (HF:H_2O = 1:100). Then, 10-nm-thick SiO_2 was formed on the substrate as a gate insulator by wet oxidation at 850°C. Then, 1.2-nm-thick N-doped LaB_6 IL was formed to control the V_{TH} of the drive OFET by RF sputtering at an RF power of 20 W at room temperature (RT) [4]. The patterning of N-doped LaB_6 IL was realized by Si wafer covering. Next, 10-nm-thick pentacene (99%, Aldrich) film was deposited by using thermal evaporation at RT with deposition rate of 0.3 nm/min through a stencil mask for isolation. Then, Au top-contact electrode was formed by thermal evaporation. Finally, Al was evaporated for V_{out} and back-gate electrodes. The device size of each OFET was L_D/W_D = 50 / 1700 μm for the drive OFET and

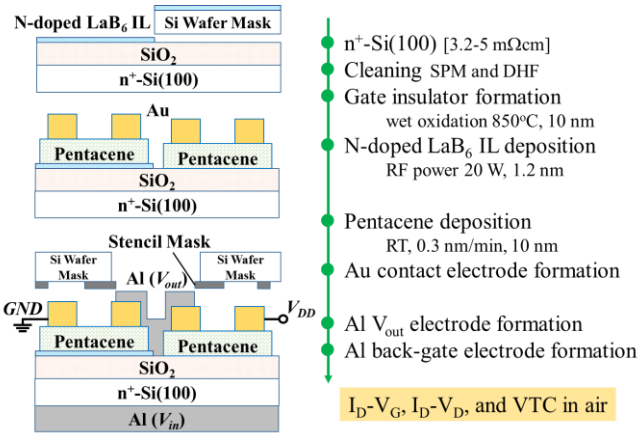

Fig. 2 Schematic cross-section of the process flow of fabricated pentacene-based pseudo-CMOS inverter with common-gate geometry.

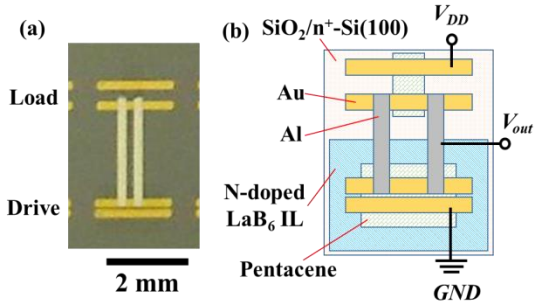

Fig. 3 (a) Top view and (b) schematic configuration of the fabricated pseudo-CMOS inverter.

L_L/W_L = 300 / 500 μm for the load OFET taking into account the channel resistance. The fabricated pseudo-CMOS inverter was evaluated by I_D-V_G, I_D-V_D, and voltage transfer characteristics (VTC) utilizing Agilent 4156C in air.

3. Results and Discussion

Figure 4 shows surface morphology of pentacene film observed by optical microscopy. The pentacene films were deposited on a 50-nm-thick SiO_2 gate insulator for easy to observe the morphology. Both pentacene films in drive and load OFETs showed typical dendritic grains, and their grain size were approximately 2–3 μm. Figure 5 shows I_D-V_G and I_D-V_D characteristics of each OFET in the fabricated pseudo-CMOS inverter. The V_{TH} of drive and load OFETs were extracted as -2.4 V and -1.3 V, respectively.

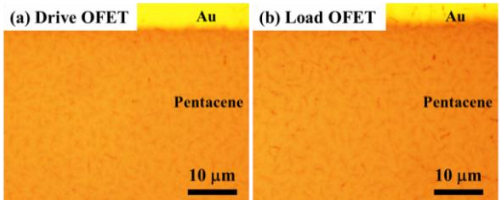

Fig. 4 Surface morphology of pentacene films for (a) drive OFET (with N-doped LaB_6 IL) and (b) load OFET (without N-doped LaB_6 IL).

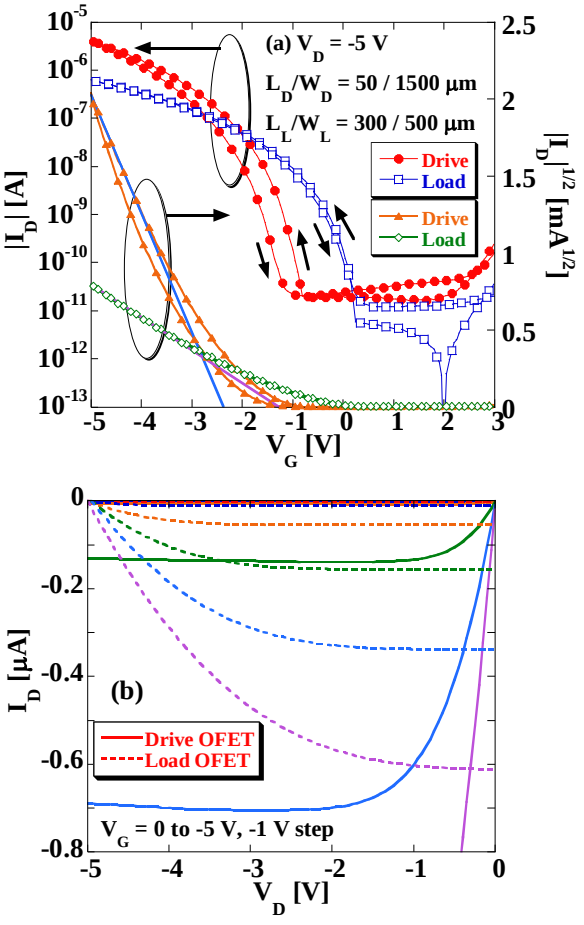

Fig. 5 (a) I_D-V_G and (b) I_D-V_D characteristics of drive and load OFETs in the fabricated pseudo-CMOS inverter.

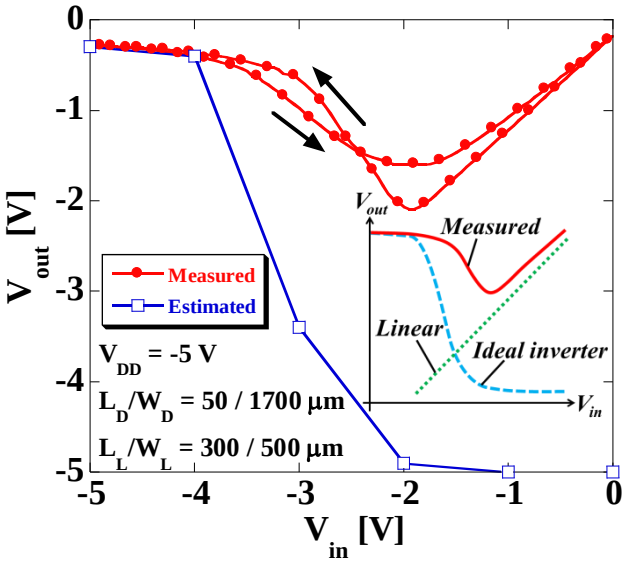

Fig. 6 VTCs measured and estimated from operation points in Fig. 5(b) of the fabricated pseudo-CMOS inverter. The inset shows speculated characteristics of measured and ideal inverter.

Figure 6 shows VTC of the fabricated pseudo-CMOS inverter. The VTC shows typical inverter characteristic by the operation voltage at -5 V, although the linear characteristic began to appear at V_{in} = -2 V or smaller, as shown in the inset of Fig. 6. Inverter characteristic was realized by V_{TH} control between load and drive OFETs with N-doped LaB_6 IL, as shown in Fig. 5(a). However, logic swing was 1.8 V, although the logic swing estimated from operation points in Fig. 5(b) was 4.7 V. This was because linear characteristic degraded inverter characteristic probably caused by small V_{TH} difference of 1.1 V. Therefore, we believe that the adequate design of V_{TH} and scaling would realize further improvement of the inverter characteristic.

4. Conclusion

In this study, we demonstrated pentacene-based pseudo-CMOS inverter utilizing N-doped LaB_6 IL. Inverter characteristic was realized of the operation voltage at -5 V even in air by introducing N-doped LaB_6 IL. Common-gate geometry of this pseudo-CMOS inverter would be suitable for the scaling, and the adequate design of V_{TH} and further scaling would improve the inverter characteristics.

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