# Electron Transport of Dopants Induced Quantum Dots in Silicon Nanowire Field Effect Transistor at Low Temperature

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## Abstract

We demonstrate the fabrication process and electron transport of quantum dots (QDs) induced by dopants in silicon nanowire field effect transistor (NW-FET) at low temperature. The spin-on dopants and thermal diffusion methods are applied to form the phosphorus dopants along nanowire. The nanowire notch design with notch structure helps to provide enhanced electrical confinement and make fabrication process be more practical. The single-electron tunneling transport through QDs is measured at 5K with Coulomb stability diagram. The Efros–Shklovskii variable range hopping (ES-VRH) electron transport mechanism has been obtained and we achieved average hopping distance of 10 nm at 300K.

# 1. Introduction

Extreme scaling and random distribution of dopants in the silicon MOSFET channel can lead to threshold voltage fluctuation and non-uniform electrical performance form device to device [1-4]. Since the nuclear spin of donor atoms in doped silicon was demonstrated they could be used for quantum information host and possibility to measure single dopant transport [5]. The electron tunneling transport through individual dopant in silicon transistor was reported initially due to the accidentally random diffused dopants in channel [6,7]. With the help of ion implantation and STM technology, the position of single atom can be precisely controlled in channel [8,9]. To make the fabrication process more compatible with CMOS technology, the new type of few dopants device with cluster of dopants induced QD was proposed [10]. However, the 5 nm ultrathin silicon device layer limits the fabrication process compatibility and tolerance.

In this work, we report the notched nanowire structure to confine the thermally diffused spin-on dopants in vertical direction without thinning the device thickness to sub-10 nm scale. We present the device low temperature characteristics with electron tunneling through dopants induced QDs and the ES-VRH transport mechanism has been obtained with temperature dependence measurement.

# 2. Device Fabrication

The device was fabricated based on p-type silicon-on-insulator (SOI) platform with 100 nm silicon and 200 nm BOX layer. The thermal oxidation was applied to thin the silicon layer to 50 nm. Then phosphorus based spin-on dopants were thermally diffused with SiO<sub>2</sub> doping mask to form source/drain and channel doping. The resulting doping concentration is  $5 \times 10^{18}$  cm<sup>-3</sup>. The notched nanowire shown in Fig. 1 (a) was formed using fluorine based plasma etch. After nanowire etch, SiO<sub>2</sub> gate oxide of 10 nm was formed by dry oxidation. The source/drain contacts were metalized by electron beam evaporated 10 nm/200 nm Ti/Al stack and lift-off process. Rapid thermal annealing was used to form the ohmic contacts. Finally, 150 nm thick Al single top gate was deposited over the notched nanowire region. The SEM image of silicon NW-FET device is shown in Fig. 1 (b).



Fig. 1 (a) SEM images of silicon notched nanowire after dry etch.(b) SEM image of final device with Al top gate over nanowire.

#### 3. Device characteristics

The low temperature electrical measurements were carried out to characterize the device performance. The device was measured using Agilent B1500 semiconductor parameter analyzer with low temperature probe station. The Coulomb stability diagram at 5K is shown in Fig. 2. The V<sub>GS</sub> is swept from 0 V to 2 V with 5 mV step and the V<sub>DS</sub> is from -2.5 mV to 2.5 mV with 0.02 mV step.



Fig. 2 Coulomb stability diagram measured at 5K showing two Coulomb diamonds. The absolute I<sub>DS</sub> value is used to create the stability plot.

When  $V_{GS}$  is lower than 0.4 V, the device is at the off state. With the increasing of  $V_{GS}$ , two Coulomb diamonds marked with dashed lines are obtained at low  $V_{DS}$  range. The significantly different shapes of diamonds suggest that the current peaks between diamonds are corresponding to different QDs [11]. Because the spin-on dopants are diffused from the center of nanowire and source/drain region, so the lateral diffusion of dopants in channel are likely to form groups of dopants. These groups of dopants within channel then exhibit QD characteristics similar to structurally formed QD.

Fig. 3 shows the temperature dependent of conductance plot under different  $V_{GS}$  values around current peaks.



Fig. 3 Measured conductance as a function of  $T^{\text{-}1/2}$  under different  $V_{GS}$  of the silicon notched nanowire device.

The black straight line indicates that the linear Log G-T<sup>-1/2</sup> relationship that follows the ES-VRH model when the temperature is in the range of 40K to 300K. The conductance equation is shown as below in eq. (1) [12],

$$G(T) = G_{ES} exp[-(T_{ES}/T)^{1/2}]$$
 (1)

The  $T_{ES}$  is the ES-VRH characteristic temperature and the value is calculated to be 484K. The parameters for hopping can be extracted from eq. (2) [12],

$$T_{\rm ES} = \frac{2.8e^2}{4\pi\epsilon_0\epsilon_{\rm r}k_{\rm B}\xi}, \ \bar{r} = \xi \left(\frac{T_{\rm ES}}{T}\right)^{\frac{1}{2}}$$
(2)

The  $\xi$  is the localization length and  $\bar{r}$  is the average hopping distance for ES-VRH. From the above equations, the localization length is extracted to be 8 nm and the average hopping distance is calculated to be approximate 10 nm when T=300K. The ES-VRH proves that the dopants in channel form localized sites for electron transport, which is similar to the observations from [13].

#### 4. Conclusions

Preliminary results of single-electron tunneling through dopant induced QDs is obtained at 5K. The electron transport behaviors are measured to follow ES-VRH mechanism between 40K to 300K. This experiment also suggests that the nanowire notch structure with spin-on dopants are adaptable to fabricate few dopants device and the formed clustered dopants can be used as QDs.

#### Acknowledgements

We would like to thank Prof. J.J.L. Morton of University College London for experimental discussion during the fabrication and measurements.

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