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Effect of the Number of Quantum Wells on SiGe/Si Based Thermistor Performance

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Abstract

This work represents the effect of number of quantum wells on silicon-germanium/silicon ($Si_{0.5}Ge_{0.5}$/Si) based intrinsic thermistor device performance. Experimental results of the thermistor prototypes with different number of quantum wells are provided in terms of temperature coefficient of resistance (TCR) and 1/f noise performance. No significant change is observed neither on the TCR performance nor the 1/f noise performance. The outcome of the study demonstrates that the use of single quantum well significantly simplifies the required epitaxy process in order to achieve high TCR and low noise performance.

1. Introduction

Uncooled microbolometers are one of the most popular technologies for the majority of commercial and military infrared imaging applications due to their advantages in terms of low-cost, low-weight and low-power dissipation [1]. They are thermal infrared sensor based on the absorption of an electromagnetic radiation and thus increase their temperature. The resulting temperature increase is a function of the radiant energy striking the bolometer and is measured with a resistance change [2].

The temperature sensing material (thermistor) has a large influence on the performance of the microbolometer. A high temperature coefficient of resistance (TCR) and a low 1/f noise constant are the two main figures of merit of a desirable material. In commercial microbolometers, Vanadium Oxide (VO_x) and amorphous silicon (a-Si:H) are used. However, their TCR performances are limited to 2-3 %/K [2]. Recently, single crystalline SiGe/Si multi quantum well (MQW) structure has attracted an increasing attention as an alternative thermistor material due to not only its noise performance but also its high TCR value obtained by the increasing Ge content [3]. The promising noise performance of SiGe/Si MQW is based on the reason of its well defined monocrystalline structure. On the other side, the higher TCR values by the higher Ge content in SiGe wells are attributed to the increasing the barrier height which results in larger number of confined energy states and the number of carriers (holes in this case). Ge% concentration effect on SiGe/Si MQW based thermistor performance has been already systematically shown in [3]. Besides that, there are few more design parameters influencing the thermistor performance such as the thickness or the number of SiGe layers in the MQW stack. By the increasing the SiGe layers thicknesses or the number; the sensitivity of the thermistor can be improved due to the increasing number of charge carriers contributing to thermal excitation process. Although the nominal resistance of these devices is reversely proportional to the number of free charge carriers and might be a challenge for a corresponding read-out circuitry of the microbolometer device, a method for tuning the resistance of highly Ge concentrated SiGe/Si MQWs is presented in [4]. In literature, there are some studies showing the effects of some processing methodologies such as silicidation and carbon incorporation on the thermistor performance with the limited Ge content [5]. Nevertheless, this paper presents the effect of number of quantum wells on SiGe/Si based MQW including 50% Ge in terms of the TCR and 1/f noise performances of a thermistor device.

2. Experimental Details

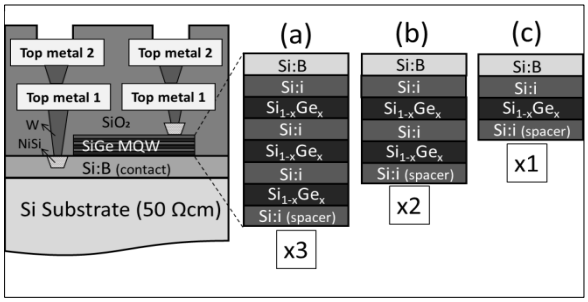

Fig. 1 Schematic of the intrinsic thermistor device and the prepared test devices with (a) three quantum well layers, (b) two quantum well layers (c) single quantum well layer.

A schematic cross-section view of the fabricated $Si_{0.5}Ge_{0.5}$/Si MQW based intrinsic thermistor device is shown in Fig. 1. The fabrication is done on an 8-inch Si (001) wafer and in a CMOS clean room environment. Epitaxial growth of $Si_{0.5}Ge_{0.5}$/Si superlattice structure is carried out using reduced pressure chemical vapor deposition system and detailed in [6]. After standard RCA cleaning followed by H_2 bake, a 500 nm B-doped Si is deposited as the

bottom contact of the device with a 250 nm spacer layer of Si on top. The active layer stack is prepared with three, two and single layer of fully strained SiGe quantum well as shown in Fig.1 (a), (b), and (c), respectively. The thickness of the quantum wells and Si barrier layers in the test devices are 10 nm and 50 nm, respectively. A 250 nm undoped Si capping and a 500 nm B-doped Si are deposited for a symmetric device behavior. The pixels are patterned for 50 µm × 50 µm pitch size. In order to realize low-ohmic contact, a self-aligned Ni silicidation is performed. Finally, the process flow is ended by a metallization and pad openings.

3. Results and Discussions

In order to investigate the effect of number of quantum wells in terms of TCR value, I-V measurements are performed over a temperature range of 278 to 323 K. The extracted TCR values for the test devices including different number of quantum well are given in Fig. 2. As seen, the observed TCR values are not significantly affected by the decreasing number of quantum wells. A slight dependence of TCR on the number of quantum wells is observed; as the number of quantum wells increases, the TCR increases. This can be explained by the more available charge carriers with the increasing number of quantum wells. It can be also due to higher resistance values of the samples with more quantum wells. In Fig. 3 increasing resistances by increasing the number of quantum wells are clearly seen.

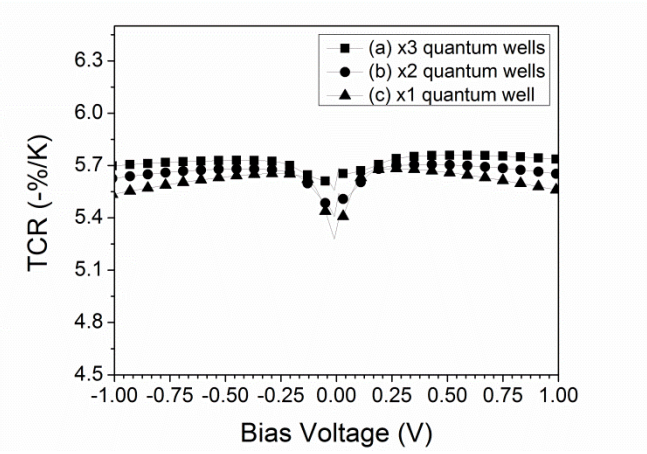

Fig. 2 TCR vs. bias voltage measured on SiGe/Si MQW structures with different number of quantum wells; (a) x3, (b) x2 (c) x1.

In Fig.4 the noise voltage power spectral densities between 1 and 10^3 Hz on the SiGe/Si MQW structures with different number of quantum wells are shown. Although it is known that there is a trade-off between increase of the number of SiGe layers and noise as a result of higher imperfections introduced by more Si/SiGe interfaces, the results in Fig. 4 show no significant effect of the quantum well numbers on the noise performance. This might be explained either with the high interface quality is still kept by the increasing number of quantum wells or the small differences in the resistance values of the samples.

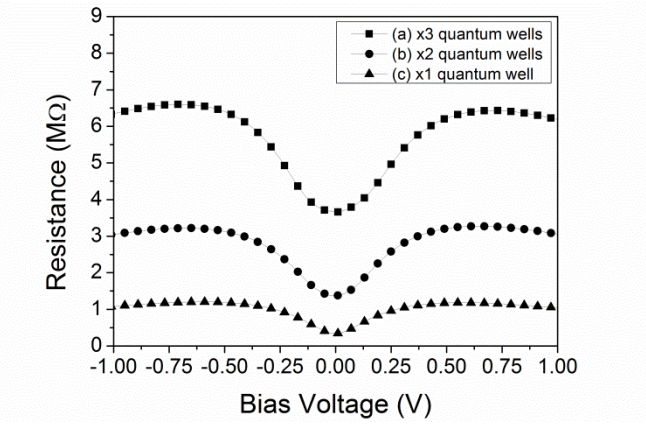

Fig. 3 Resistance-voltage characteristic on SiGe/Si MQW structures with different number of quantum wells; (a) x3, (b) x2, (c) x1.

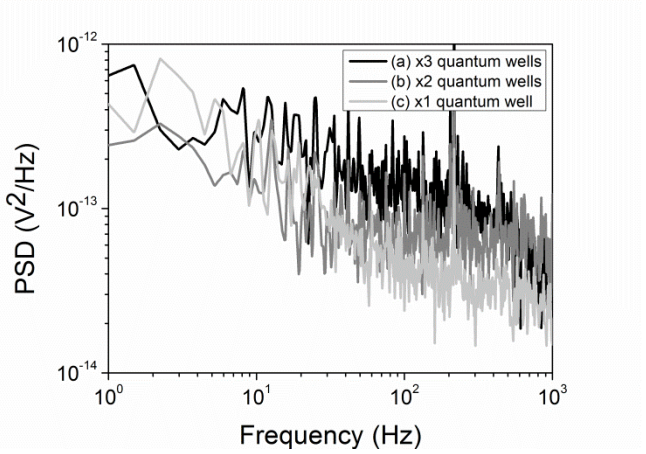

Fig. 4 Power spectral density of noise voltage vs. frequency measured at 0.66 V for SiGe/Si MQW structures with different number of quantum wells; (a) x3, (b) x2, (c) x1.

4. Conclusions

In this study, an effect of number of quantum wells on $Si_{0.5}Ge_{0.5}$/Si based thermistor performance is presented. No significant drop of the thermistor performance is observed with single quantum well compared to the others. This is also good if the epitaxy process complexity is considered, because limited thermal budget is required for Si growth after the first SiGe growth to maintain crystal quality of SiGe. The results clearly show the potential of single SiGe quantum well as a thermistor material with a significant advantage of easier process integration, high throughput and low cost.

References

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