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Device Characteristics of Nano Scale Junctionless Accumulation Mode FET (JAM-FET) with Localized Anti-channel Doping

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1. Introduction

Traditional immersion mode (IM) MOSFET device requires sharp PN junction to achieve the source/drain region and to reduce the channel length variation [1]. When CMOS technology scaling down, the traditional IM MOSFET device requires the ultra-sharp (USH) source/drain (S/D) junction profile in channel region [2]. But the USH junction formation is difficult [2-4]. Recent years, devices without PN (or NP) S/D-channel junction have been used to overcome this issue, which is the junctionless FET (JLFET) or junctionless accumulation mode FET (JAM-FET) [5-7]. The JLFET presents the simple device process and more precise channel length [7-10]. Thus, the JLFET is one of the most promising candidates for the next generation of CMOS device application [11]. But, the JLFET is turned off by the depletion region in channel below the gate electrode. Using large work function difference between the gate and Si-channel to achieve the appropriate threshold voltage for JLFET [5]. In order to improve the I_{ON} current, the Si-channel requires high doping to increase the majority carriers and reduce the channel resistance. But this leads to increase the I_{OFF} current due to the small depletion region. In the other hand, reducing the channel doing could reduce the I_{OFF}, but the I_{ON} current is also decreased. Thus, optimum channel doping profile with large I_{ON}/I_{OFF} ratio and appropriate channel thickness are the key roles for the JLFET (JAM-FET) device design [12-15]. In this study, a localized anti-channel doping below the gate sidewall is proposed to improve the device characteristics of JAM-FET. Additionally, the n- and p-type JAM-FET devices w/ and w/o anti-channel doping are also compared and studied.

2. Experimental

A 6-in p-type Si wafer is used for the JAM-FETs fabrication. Firstly, the buried oxide (200 nm) and LPCVD Si_3N_4 (50 nm) were formed. Then, the amorphous Si (30 nm) was deposited and to form the Poly-Si channel by the solid phase crystallization (SPC). N- and p-type channel doping of phosphorus and BF_2 ions, respectively, with 1×10^{14} dose/cm^2 and the RTA process for the dopant activation. The active area was defined by the E-beam lithography and RIE etching. Then, the gate dielectric is the ALD Al_2O_3 (3.5 nm). The metal gate is PVD TiN (50 nm), and the gate area is defined by the 2nd E-beam lithography. The anti-ions-channel doping is formed by using the BF_2 and As ions of 2×10^{13} dose/cm^2 with a tilting angle of 45° to form the N^- and P^- regions below the gate sidewall for the n- and p-type JAM-FET devices, respectively. After spacer formation, a high same channel type doping was proceeded to form the S/D region. Finally, the PVD Al-Si-Cu metal (200 nm) was as the contact metal. The schematic of JAM-FETs and the detail process are shown in **Fig. 1** and **Fig. 2**, respectively.

3. Results and Discussion

Fig. 3 and **Fig. 4** show the I_{DS}-V_{GS} curves of n- and p-type JAM-FETs, respectively, w/ and w/o anti-channel doping for W/L= 40/80 nm. The devices with anti-channel doping reveal the better performance, including the small I_{OFF} and large I_{ON}/I_{OFF} ratio for n- and p-type JAM-FETs. The I_{ON} is also decreased for device with anti-channel doping, but it is acceptance for the low power application. In addition, the p-type JAM-FET with anti-channel doping **(Fig. 4b)** reveals better characteristic than that of the n-type JAM-FET. From the inset of the **Fig. 3** and **Fig. 4** related to the device performance of the subthreshold swing (SS) and the drain induced barrier lowering (DIBL), the anti-channel doping devices present the better characteristics. **Fig. 5** and **Fig. 6** show the I_{DS}-V_{DS} curves of n- and p-type JAM-FETs, respectively, w/ and w/o anti-channel doping. For n-type device with anti-channel doping (**Fig. 5b**), the drain current is reduced and the I_{DS} curve presents the linear parasitic resistance behavior especially for the V_{GS} >1.2V. This indicates the anti-channel doping below the gate sidewall destroy the origin channel doping profile in the bulk channel, resulting in the channel concentration decreased obviously. In addition, the p-type JAM-FET with anti-channel doping in **Fig. 6b** shows the smaller decrease of drain current (from 9.50 to 2.71 μA) than that of the n-type JAM-FET (from 3.85 to 0.526 μA), and there is smaller linear parasitic resistance behavior at large V_{GS} voltage (-2.0V). Presumably, the anti-channel doping ions (As) of p-type device is more weight than that of BF_2 ions of the n-type device, leading to the anti-channel doping did not implant deeper into the bulk channel and located near the surface below the gate sidewall. Thus, the P^- region is formed near the surface region of channel below the gate sidewall, resulting in the better I_{DS}-V_{DS} performance. **Fig. 7a** shows the comparison of I_{DS}-V_{GS} curves of n-type JAM-FET for the devices w/ and w/o anti-channel doping. There is larger reduction on I_{OFF} compared with the I_{ON} (reduced to 0.062 vs. 0.101 times). For the I_{ON} current of I_{DS}-V_{DS} curve, the I_{ON} was decreased by 0.14 times (at V_{GS}=2.0V, V_{DS}=2.5V) compared with the device w/o anti-doping (**Fig. 7b**). In addition, the p-type device shows the smaller reduction of I_{OFF} and I_{ON} (reduced to 0.21 and 0.27 times, respectively) in **Fig. 8a**. The I_{ON} of I_{DS}-V_{DS} is reduced to 0.42 times shown in **Fig. 8b**. In summary the p-type device reveals the better anti-channel doping process. **Table I** summarized the n- and p-type JAM-FET w/ and w/o anti-channel doping. The anti-channel doping can improve the SS, DIBL, and I_{ON}/I_{OFF} ratio, but the drain current is degraded.

4. Conclusions

The anti-channel doping near the gate sidewall will improve the performance of the SS, DIBL, and I_{ON}/I_{OFF} ratio. But the driving current will be degraded. Thus, the appropriate anti-ions concentration and the implanted energy are the important parameters to achieve the optimum device performance with good driving current.

Acknowledgements

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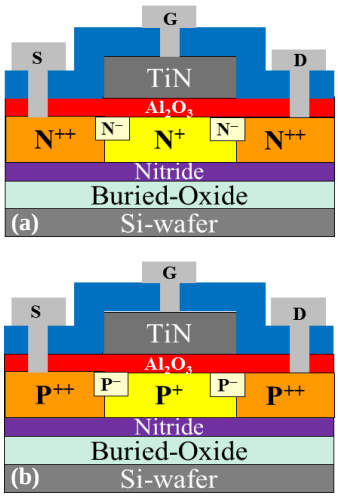


Fig.1 Schematic structures of (a) n-type and (b) p-type channel Junctionless accumulation mode FET (JAM-FET) transistors with anti-channel doping.

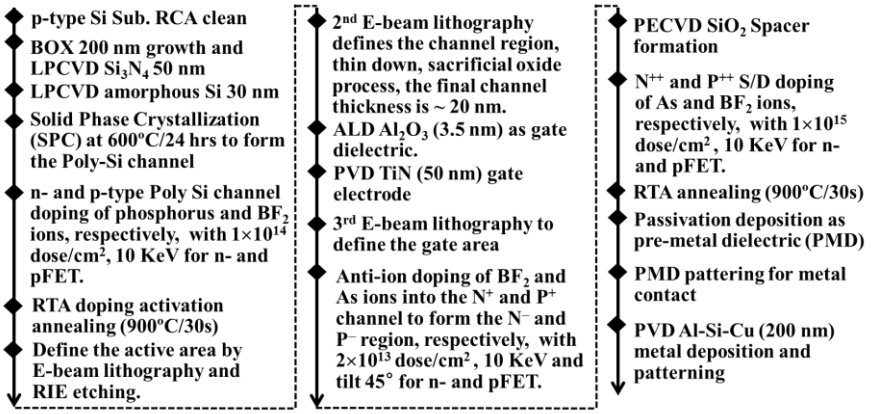


Fig.2 Fabrication process and deposition conditions for the n- and p-type Junctionless accumulation mode FETs with anti-channel doping. Without anti-channel doping JAM-FETs are also prepared for the comparison.

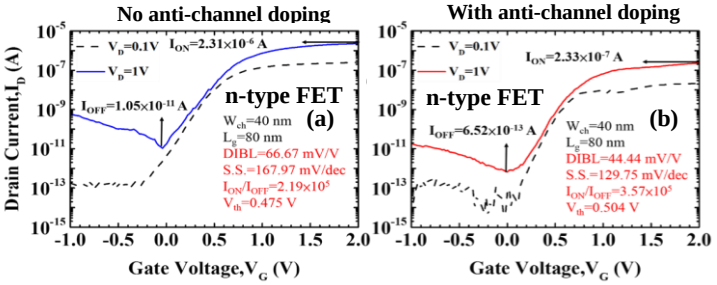


Fig.3 I_{DS}-V_{GS} curves of **n-type** JAM-FETs (a) without anti-channel doping, and (b) with anti-channel doping for the device dimension of W/L = 40/80 nm. The I_{ON}/I_{OFF} ratio is calculated by the I_{DS}-V_{GS} curve at V_{DS}=1.0V

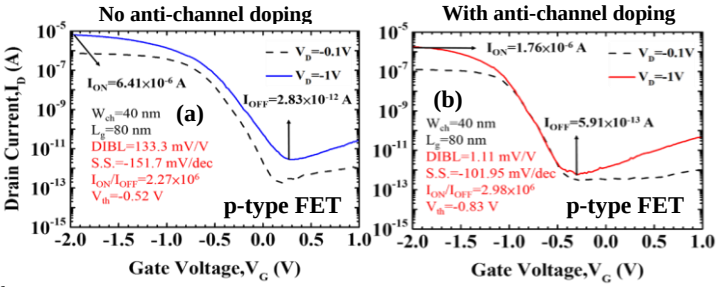


Fig.4 I_{DS}-V_{GS} curves of **p-type** JAM-FETs (a) without anti-channel doping, and (b) with anti-channel doping for the device dimension of W/L = 40/80

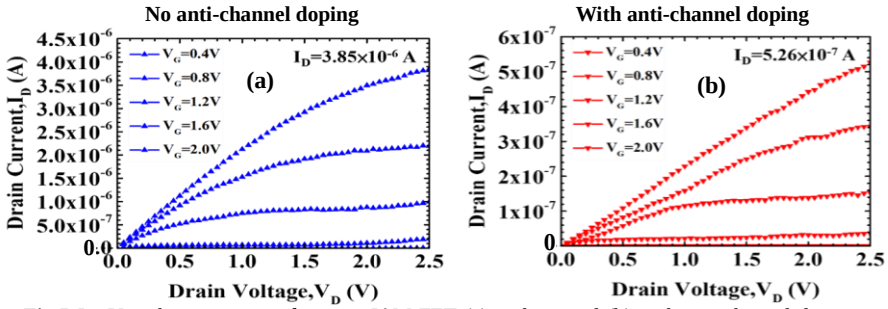


Fig.5 I_{DS}-V_{DS} characteristics of **n-type** JAM-FET (a) without and (b) with anti-channel doping for the device dimension of W/L = 40/80 nm.

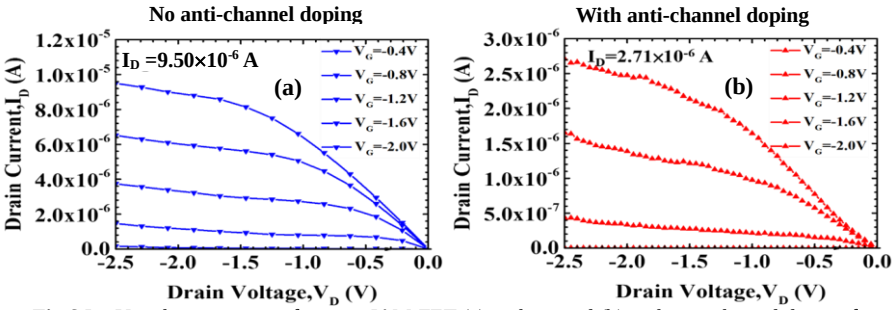
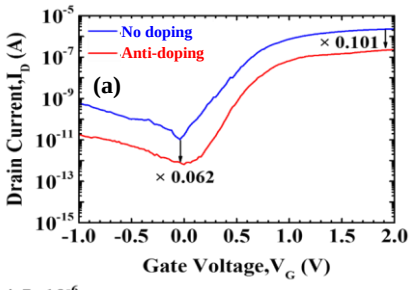


Fig.6 I_{DS}-V_{DS} characteristics of **p-type** JAM-FET (a) without and (b) with anti-channel doping for the device dimension of W/L = 40/80 nm.



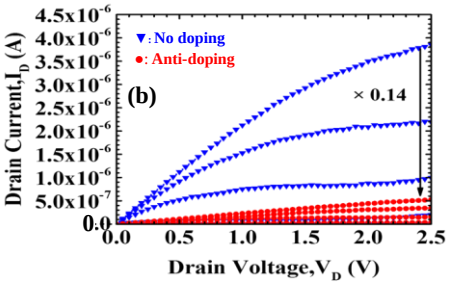


Fig.7 (a) I_{DS}-V_{GS} and (b) I_{DS}-V_{DS} characteristics of **n-type** JAM-FET with and without anti-channel doping for the device dimension of W/L = 40/80 nm.

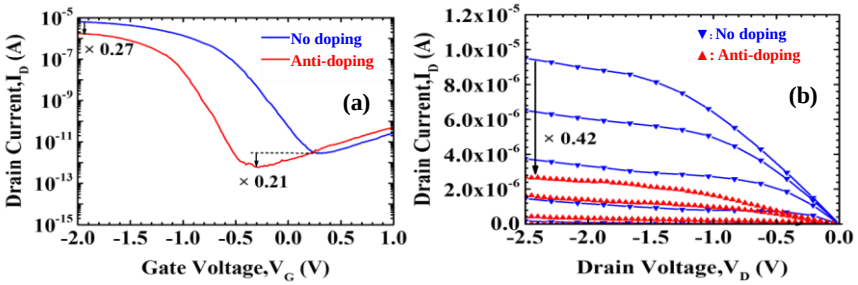


Fig.8 (a) I_{DS}-V_{GS} and (b) I_{DS}-V_{DS} characteristics of **p-type** JAM-FET with and without anti-channel doping for the device dimension of W/L = 40/80 nm.

Table I Device performance of n-type and p-type JAM-FET w/ and w/o anti-channel doping for W/L= 40/80 nm.

Device Performance	No doping	Anti-channel doping	No doping	Anti-channel doping
	n-type FET	n-type FET	p-type FET	p-type FET
SS (mV/dec)	167.97	129.75	-151.70	-101.95
DIBL (mV/V)	66.67	44.44	133.30	1.11
I_{ON}/I_{OFF} ($\times10^5$)	2.19	3.57	22.70	29.80
$I_{DS,sat}$ (μA) ($\lvert V_{GS}\rvert$=2V, $\lvert V_{DS}\rvert$=2.5V)	3.85	0.53	9.5	2.71
V_{th} (V)	0.48	0.50	-0.52	-0.83