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Impact of quantum dot characteristics on the hybrid SET-FET circuit behavior

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Abstract

Quantum dot (QD) is a core element of single electron transistors. The variability of the QD characteristics can affect the behavior of the hybrid SET-FET circuit. We have developed a new SET compact model able to simulate the influence of variations of QD properties in a new SET concept based on vertical nanowires.

1. Introduction

Single-electron transistors (SETs) are key elements for low-power and high-integration density electronics. Its main special feature is the channel concept, based on a conductive island or quantum dot (QD). When SET QD is large, the device can only operate at low temperatures, but by reducing the QD below 4 nm single-electron effects, as Coulomb blockade (CB) oscillations, can be observed at room temperature [1]. SET current exponentially depends on the tunneling barrier thickness, what implies that a good control of QD characteristics, e.g. size and position, is required. SET devices show significant benefits, among them low power consumption; but several limitations threaten their feasibility, as background charge noise, low drive current, device stability and ultra-low temperature operation. Silicon-based SET arises as a promising candidate, because it reduces the random charge near the SET island [2], minimizing the background charge noise. The co-integration with a MOSFET can improve the SET low output current, because the FET would amplify it. The hybrid circuit is proposed as a feasible candidate to extend the usefulness of SET for VLSI circuits beyond 10 nm node [3]. In a previous work [4] we have shown the co-integration of vertical nanowire (NW) FET with a SET presents an optimal behaviour.

2. Simulations benchmark

We investigate a new concept of SET implementation based on a vertical silicon pillar (d_{pillar} =10 nm) with an embedded SiO_2 layer (Fig. 1.a). A silicon nano-dot is introduced by ion beam mixing and subsequent annealing [2]. SET structure and behavior have been evaluated by 3D simulations based on quantum mechanical calculations using nextnano++ simulator and self-developed post-processing software [5]. The 3D simulations for silicon pillar SETs cannot be described properly by SET compact models from literature (e.g. [1]), which are usually derived for idealized metallic structures. We have developed a new compact model for silicon-based SETs, which takes into account the effect of the QD band gap. For the individual current peaks we employ the equations derived by Inokawa et al. [1], but restrict the oscillations to gate voltages above a threshold voltage as shown in Fig. 2a. Close to the threshold we use an exponential damping term to model the reduced peak height observed in 3D simulations. Further, the position of the first peak is shifted to positive gate voltages, which is due to a difference in the shape of the electrostatic potential for the uncharged QD in comparison to the charged one. The compact model has been implemented for HSPICE [6].

Variability is a relevant reliability topic at nano-meter regime [4]. We have analysed the effect of applying a 10% variation for the main QD characteristics. We calibrated the model to a set of 3D simulations, where we have varied geometrical properties as well as external quantities like temperature and voltages. From these calibrations we have derived a set of empirical equations that describe how the model parameters depend on the varied quantities. This allows the modification of several QD characteristics directly within the compact model (Fig. 1.b): a) position (z_{dot}), b) size (d_{dot}) and c) gate-to-pillar distance (t_{gp}). We have simulated the NW-FET device by using BSIM model [7] at their nominal conditions. From the HSPICE simulations [6] we have characterized the SET-FET behaviour by obtaining the maximum output current ($I_{D,SET-FET}$) and the amplitude of the CB oscillations (h_{ID}= $I_{D,max}/I_{D,min}$), which highlights the SET relevance within the hybrid circuit.

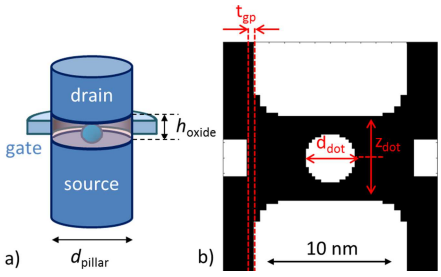

Fig. 1 Schematic of: a) silicon-based SET pillar with embedded SiO_2 layer; and b) QD characteristics description.

Fig. 2.b shows the amplification effect in a SET-FET circuit. The low current level at the SET output ($I_{D,SET}$), is exponentially amplified at the hybrid circuit output ($I_{D,SET-FET}$). Inset of Fig. 2.b presents the schematic of a SET-FET, which is composed of two devices (SET and FET), a current source (I_{BIAS}) and a voltage source (V_D) [3].

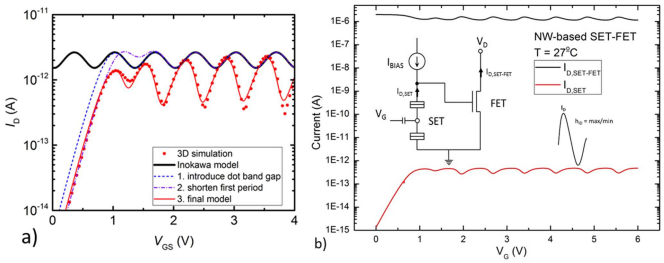

Fig. 2 a) Comparison between 3D and HSPICE simulations with different stages of the SET compact model. b) $I_{D,SET}$ and $I_{D,SET-FET}$ of a NW-based SET-FET. The inset shows the hybrid circuit schematic and h_{ID} relation.

3. Influence of the QD variations on SET-FET circuit

Fig. 3 presents how the QD characteristics affects the behavior of a single SET, when z_{dot} (a), d_{dot} (b) and t_{gp} (c) are shifted away from their nominal position (z_{dot}=0 nm, d_{dot}=3.2

nm and t_{gp}= 0.7 nm). The largest $I_{D,SET}$ is obtained when the QD is centered within the oxide layer (Fig. 3.a) and with the largest QD size (Fig. 3.b), due to the minimized tunneling junctions. The gate-to-pillar distance variation has a negligible influence on I_D and h_{ID}, but larger impact (15%) on the SET CB oscillations period, which depends on e/C_G [3].

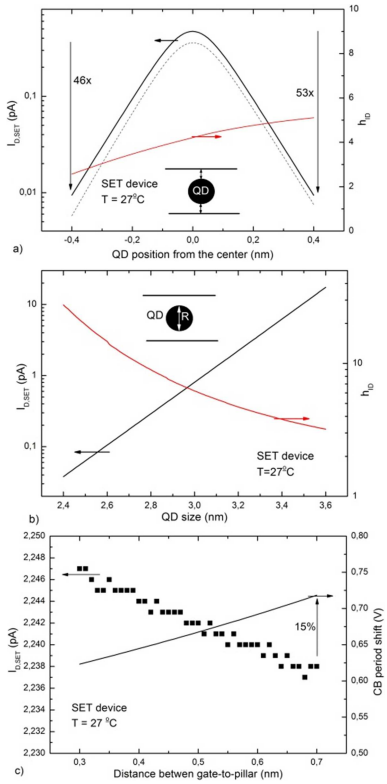

Fig. 3 Impact of the QD characteristics, a) z_{dot}, b) d_{dot} and c) t_{gp}, on the performance of a single SET.

QD variations also affect SET-FET output behavior. Figs. 4 show the impact of the QD characteristics variation on the hybrid circuit. In contrast to single SET results, the hybrid circuit exhibits the lowest $I_{D,SET-FET}$ value at the oxide layer center (Fig. 4.a). This behavior is related to the constant I_{BIAS}; when the QD is shifted away from the center, $V_{D,SET}$ increases in order to compensate for the higher tunneling resistance (Fig. 4.d). This enlarges $V_{G,FET,}$ and hence $I_{D,SET-FET}$. Fig. 4.b shows that the largest size implies the lowest $I_{D,SET-FET}$. Similar to the single SET behavior, a negligible impact on $I_{D,SET-FET}$ is observed for t_{gp}, but larger relevance is obtained for the CB oscillation (Fig. 4.c). h_{ID} shows the maximum vale close to the nominal QD values.

Finally, Fig. 5 depicts the device variability influence on the hybrid circuit when variability is focused on SET (QD characteristics) and FET (V_T) parameters shift. The highest variability is obtained for the QD size variation.

4. Conclusions

A compact SET model has been developed and applied to a novel SET implementation concept based on a vertical nanowire. The model was calibrated to 3D simulations of the SET at room temperature to obtain a realistic set of model parameters. The calibrated model allows modifying the QD characteristics, what enables the study of the impact of geometric SET variations at circuit level. The variability of the device in terms of QD variation has been simulated in the case of a single SET device and a SET-FET circuit.

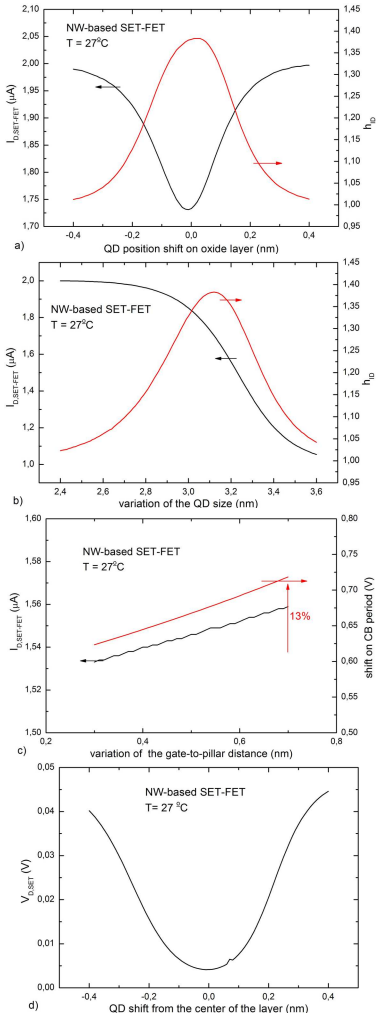

Fig. 4 Relevance of the QD characteristics, a) z_{dot}, b) d_{dot} and c) t_{gp}, into the SET-FET circuit behavior. d) Evolution of $V_{D,SET}$ when QD position shifts away from the oxide layer centre.

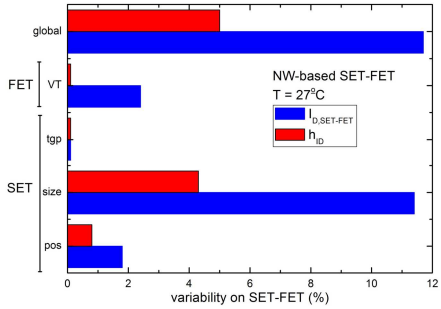

Fig. 5 Impact of the device variability, when QD characteristics (z_{dot}, d_{dot} and t_{gp}) and $V_{T,FET}$ are individualy considered.

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