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A Fast Transient Response and High Current Efficiency Output-Capacitorless Low-Dropout Regulator for Low-Power SoC Applications

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Abstract

This paper proposed a fast transient response and high current efficiency output-capacitorless low-dropout regulator (LDO). The proposed slew rate enhancement circuit is activated only when the output voltage is instantaneously changed due to the transient of the load current. This method not only can instantaneously increase the bias current source current, to achieve rapid recovery of the output voltage, the load regulation to get better performance, but also can reduce power consumption. Based on a 0.18-μm standard CMOS process, measurement results showed that the proposed LDO can operate from 1.2 V to 1.8 V with an output voltage of 1 V, and can provide loading current from 3 mA to 100 mA. The current efficiency is 99.96% when operating at a maximal load current of 100 mA.

1. Introduction

As the advanced of the consumer electronics, derived various intelligent communication devices, changed people's habits of using smart devices drastically. In order to increase the endurance of the electronic devices, except increasing the batter or energy reliability, system-on-a-chip (SoC) had also become the trend of technology advancing. Since there are many different modules on the SoC system, multiple different voltage levels of DC supply voltages with are needed. Because of the smaller chip area and the easiness of design, the output-capacitorless LDOs had been widely used in RF, analog, and digital circuits [1]-[5]. However, fast transient response, small spike output voltage, high current efficiency, and low quiescent current are critical for the output-capacitorless LDOs, and these features are difficult to achieve simultaneously. In this paper, a LDO without output capacitors is proposed to effectively solve the problem of large external capacitor chips. In addition, the proposed LDO has fast transient response and high current efficiency performances.

2. Proposed Output-Capacitorless LDO

The block diagram of the proposed output-capacitorless LDO, as shown in Fig. 1. It consisted of gain stage, slew rate enhancement (SRE) circuit, and the output stage. The gain stage consisted of flipped voltage follower (FVF) [6]. The slew rate enhancement consisted of comparator, driving circuit, and R_S, C_C, and C_M for coupling the output voltage while the load current changes dramatically. The power POMS, M_P as pass transistor offered the load current. The circuit diagram of proposed LDO, as depicted in Fig. 2(a). The transistors M_{F2}, M_{F5}, M_{F6}, M_{F10}, M_{B6}, and M_{B9} consisted a common gate differential amplifier, and transistors M_{F3}, M_{F4}, M_{F8}, and M_{F9} consisted a non-inverting amplification stage with boosting gain. A Class-AB output was generated through M_{F3} and M_{F9} to drive the gate of M_{F3} which determined the charging ability of M_P; conversely M_{F9} determined the discharge capacity of M_P. M_{B1}~M_{B9} offered a reference voltage to the system. The comparator and amplifier consisted of M_{S3}, M_{S4}, M_{S5}, M_{S6}, and M_{S9}, controlled the compensation time of driving circuit. Fig. 2(b) shows that when load current from low to high at transient, due to the limited loop bandwidth and large equivalent capacitances at gates, the error amplifier which used to be operating under low quiescent current could not react to turn on the pass transistor, caused the output voltage undershoot. At this time, the capacitor, C_M coupled output voltage into error amplifier that made pass transistor turned on which could improve the spike voltage at undershoot. Conversely in Fig. 2(c), while load current from high to low, the amplifier was too hard to drive pass transistor that made the transistor could not react to turn off which cause the overshoot spike voltage was generated at output voltage. Besides coupling the output voltage to error amplifier by capacitor, C_M, driving circuit also turn on to assisted with pass transistor to turn off. The compensation signal generated from error amplifier and comparator that transfer to drive circuit to pull down the overshoot spike voltage fast and accurately.

3. Experimental Results

Fig. 3 shows the die photo of the proposed LDO and the core area is 0.028 mm^2. The transient response at 1.2 V input voltage with 1 V output under the load current from 3 mA to 100 mA, which rise time and fall time are both 0.1 μs, as shown in Fig. 4. The measured load regulation is 0.126 mV/mA, as shown in Fig. 5. Table I shows a comparison of the performances of recently developed output-capacitorless LDOs using 0.18-μm process technology.

4. Conclusions

This paper proposes a fast transient response and high current efficiency output-capactiorless LDO with a large load current range 3 mA to 100 mA. The voltage spike of undershoot is within 133 mV, and the voltage spike of overshoot is within 117 mV. The measured line regulation and load regulation are 1.24 mV/V and 0.126 mV/mA, respectively. The proposed LDO takes the advantages of fast transient response, small spike output voltage, and high current efficiency. Therefore, it is suitable for low-power SoC applications.

Table I The Comparison with Previous Works

Parameters	ISOCC'16 [1]	TPEL'16 [2]	TPEL'16 [3]	ISOCC'15 [4]	SOCC'15 [5]	**This Work**
Technology (μm)	0.18	0.18	0.18	0.18	0.18	**0.18**
Chip Area (mm^2)	0.033	0.037	0.07	N/A	0.023	**0.028**
V_{IN} (V)	1.8	1.4	1.4	1.2	1.2-1.8	**1.2-1.8**
V_{OUT} (V)	1.5	1.2	1.2	1	1-1.6	**1**
I_Q (μA)	60	0.8-154	0.61-141	161	14	**20-60**
$I_{OUT(MAX)}$ (mA)	50	100	100	100	100	**100**
Line Regulation (mV/V)	0.52	10	0.6	0.95	N/A	**1.24**
Load Regulation (mV/mA)	0.0021	0.1	0.27	20	0.0278	**0.126**
ΔV_{out} (mV)	62	52	110	36.8	343	**10**
ΔI_{out} (mA)	50	100	99.99	100	99.5	**99**
Edge Time Δt(μs)	1	1	1	1	1	**0.1**
Edge Time Ratio K	10000	10000	10000	10000	10000	**1000**
Setting Time (μs)	N/A	4	N/A	6	N/A	**0.33**
FOM	0.744	0.004-0.800	0.006-1.551	0.592	0.482	**0.004**

$$K = \frac{\Delta t \text{ used in the measurement}}{\text{the smallest } \Delta t \text{ among the designs for comparison}} \qquad FOM = K\left(\frac{\Delta V_{OUT} \cdot I_Q}{\Delta I_{OUT}}\right)$$

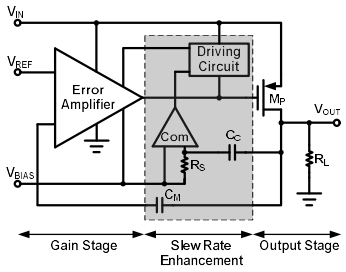

Fig. 1. Block diagram of the proposed LDO.

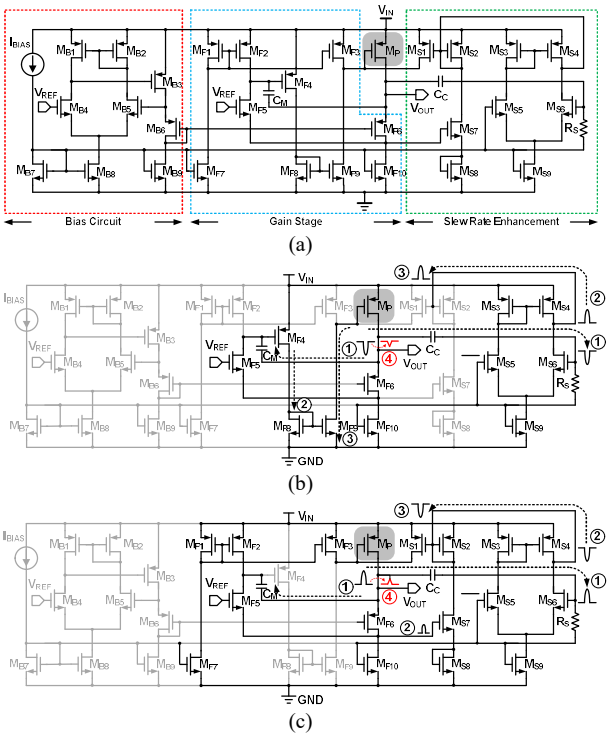

Fig. 2. (a) Circuit diagram of proposed LDO. (b) Operated under undershoot. (c) Operated under overshoot.

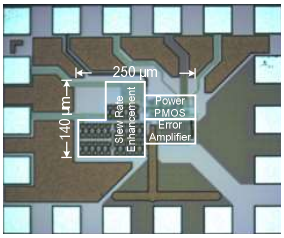

Fig. 3. Die photo of the proposed LDO.

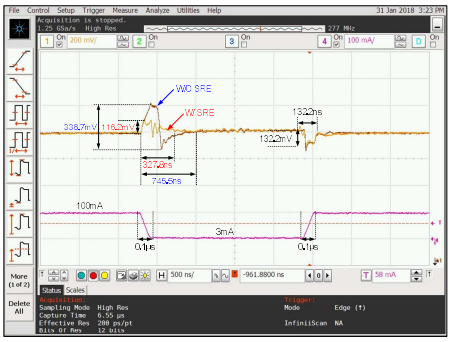

Fig. 4.The transient response of the proposed LDO.

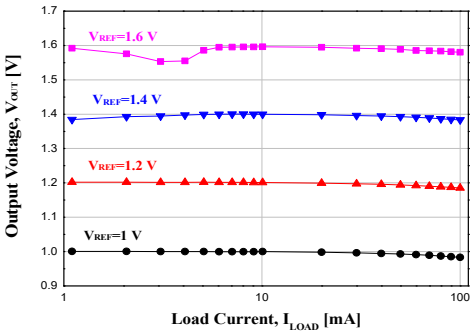

Fig. 5. Load regulation of the proposed LDO.

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