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N^+/P Hybrid Poly-Si Shell Structure Junctionless Field-Effect Transistors by Electron Beam Lithography Dosage Adjusted Method

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Abstract

This work introduces the method which used single mask by different lithography dosage to implement N^+/P hybrid nanowires shell structure N^+ channel junctionless field-effect transistors (NW shell JL-FET). The NW shell JL-FET exhibits the superior electrical properties, including high ON/OFF current ratio (>6×10^6) and steep subthreshold slope (95 mV/dec.). This NW shell JL-FET is simple to fabricate and highly favorable for use in advanced three-dimensional (3-D) stacked ICs applications.

1. Introduction

Recently, the junctionless field-effect transistor (JL-FET), which is doping high concentration and constant throughout the channel and source/drain (S/D) regions, is able to conquer the short channel effect(SCE)[1],[2]. Owing to turn-off the JL-FET architecture, the multi-gate structure and ultra-thin body (UTB) are the candidate to achieve the full depletion region at off-state[3],[4]. In addition, the hybrid channel which reduces the effective channel thickness has a remarkable performance and is capable of extending the generation of silicon as a channel material to the coming technology node[5]. Afterward, this work mentions a highly scalable hybrid N^+/P channel which is able to integrate into M3D providing worthy information for the practical industrial applications.

2. Experiment

Fig.1(a) shows the fabrication process flows of the NW shell JL-FET with the shell structure. First, 40-nm-thick poly-Si film is formed. Then, a poly-Si layer was implanted BF_2 ions at a dose of 2×10^{14} cm^{-2}. Next, the dopant was annealed at 600℃ for 4hrs. The first active layer, serving as a p-type substrate, was defined by e-beam lithography (EBL) with dosage = 5.0 μC/cm^2 and transferred by reactive-ion etching (RIE). Subsequently, the second active layer was deposited by 20 nm in-situ doped N^+ poly-Si as a channel. EBL patterned again with the same mask as the first active layer but different dosage = 5.6 μC/cm^2. Furthermore, another structure called planar shell JL-FET also forming the same process but using a different dosage of EBL patterning. Next, SiO_2 was grown as the gate oxide. Then, in-situ doped N^+ poly-Si was formed as a gate electrode, then patterned by EBL and RIE. Finally, passivation and metallization are formed.

3. Results and Discussion

Fig. 2(a-b) present an illustration of the device structure and cross-section of the channel, indicating the B-B' direction from the source side to the drain side. The A-A' direction shows the cross section of NWs perpendicular to the gate direction of the device. Fig. 2(c-d) show the top view SEM image of the NW and planar shell with gate length = 3.8 μm. Fig. 3 presents the transmission electron microscopic (TEM) image along gate direction. The figure reveals that the N^+ channel dimensions of each NW are 5.8 nm high × 112 nm wide and the p-type substrate dimensions are 17.8 nm high.

Fig. 4(a) presents the I_D-V_G curves of the NW and planar shell JL-FET at V_D = 1 V, respectively. The subthreshold slope (SS) of the NW shell JL-FET and planar JL-FET are 95 mV/dec and 156 mV/dec, respectively. Obviously, the NW device has superior ON/OFF current ratio (6×10^6) than planar shell JL-FET. Fig. 4(b) compares the DIBL characteristics of the NW shell and planar shell at V_D= 0.5V and V_D= 3V. The DIBL values of the NW and planar shell JL-FET are 50 mV/V and 91 mV/V, respectively. Where V_{TH} refers to the gate voltage at I_D = 10^{-8} Å. Fig. 5 plots the transfer I_D–V_G characteristics and transconductance (Gm) of the NW shell and planar shell at V_D = 0.1 V. The Gm of the NW and planar shell JL-FET are 18.8 nS and 36.8 nS. The NW and planar shell maximum field-effect mobility 2.4 cm^2/Vs and 1.3 cm^2/Vs, respectively. Fig. 6 compares the I_D-V_D output characteristics of the NW and planar shell JL-FET for L_G = 3.8 μm. NW device has higher saturation current than planar device because of the better channel control capability. Fig. 7(a-b) show temperature dependence on I_D-V_G curves of the NW and planar shell JL-FET on a temperature at V_D = 1 V from 50℃ to 200℃, varied in steps of 25℃. The results exhibit positive variation with increasing temperature.

4. Conclusion

This study compared the performance of NW shell JL-FET and planar shell JL-FET. The performance of the NW shell JL-FET is superior with the SS (95mV/dec.) and the high current ratio (>10^6). Furthermore, the reliability of the device is revealed the NWs shell JL-FET is convenient for a circuit design for use in a wide range of temperatures. The proposed N^+/P hybrid JLFETs with shell structure are not only easy to fabricate but also has excellent characteristics for three-dimensional (3-D) stacked ICs applications.

Acknowledgments

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References

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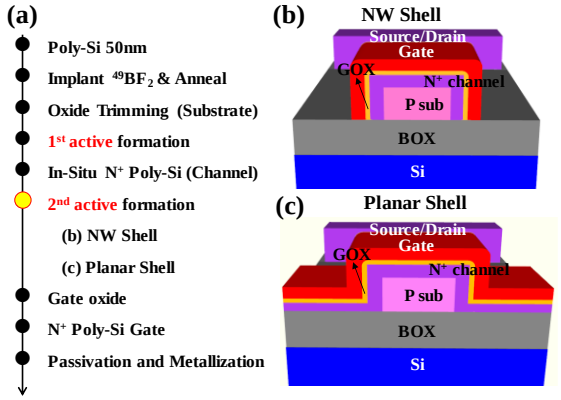

Fig. 1. The device structure for hybrid shell JL-FET. (a) The process flows of the fabrication in the shell JL-FET. (b) The cross-section of Nanowires shell. (c) The cross-section of Planar shell.

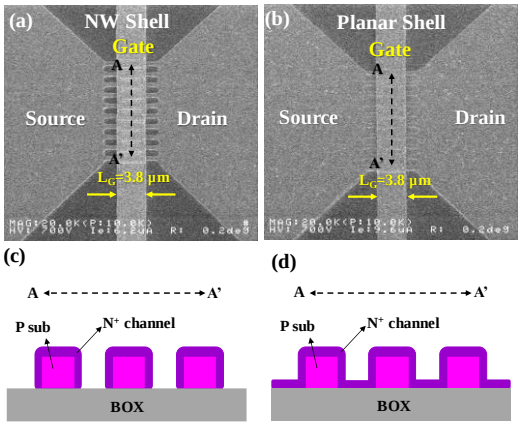

Fig. 2. Top-view SEM image of (a) the NW JL-FET and (b) the planar JL-FET with gate length = 3.8 μm. The schematic diagrams of top-view and cross-section of (c) the NW JL-FET and (d) the planar JL-FET. A-A' direction indicates the region of the channel, and B-B' direction indicates cross-section from source to drain.

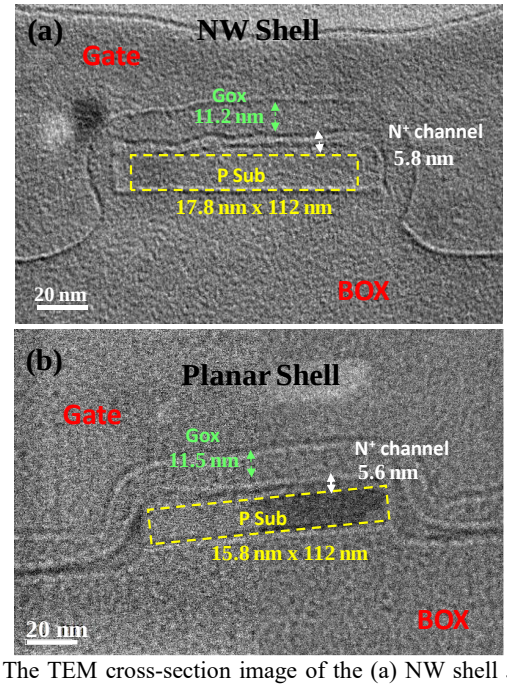

Fig. 3. The TEM cross-section image of the (a) NW shell JL-FET and (b) planar shell JL-FET along AA' direction for single nanowire structure.

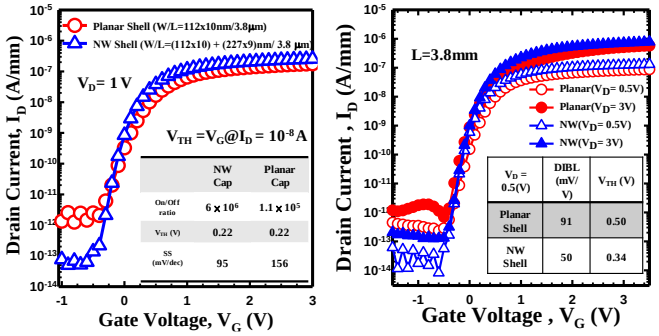

Fig. 4. (a)The I_D-V_G curves of the NW shell JL-FET and planar shell JL-FET with gate length = 3.8 μm. (b) Comparison of I_D-V_G curves of the NW shell JL-FET and planar shell JL-FET at V_D = 0.5 V and V_D = 3 V. V_{TH} is defined as the gate voltage at I_D=10^{-8}A.

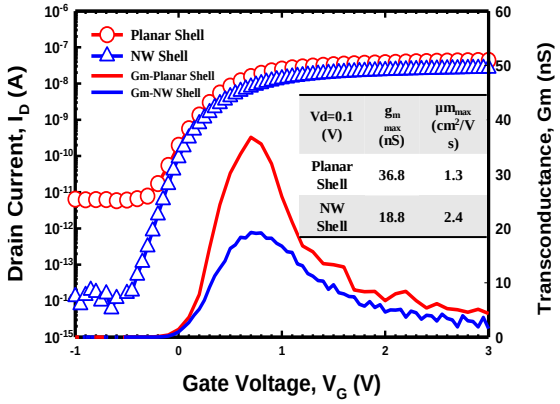

Fig. 5. Comparison of I_D-V_G curves and transconductance (G_m) of the NW shell JL-FET and planar shell JL-FET at V_D = 0.1 V. The inserted plot shows mobility values.

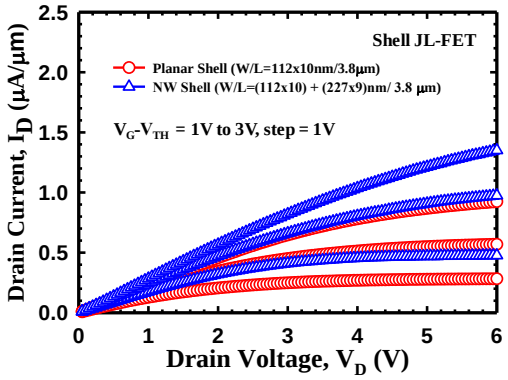

Fig. 6. I_D-V_D curves of NW and planar shell JL-FET with L_G=3.8μm.

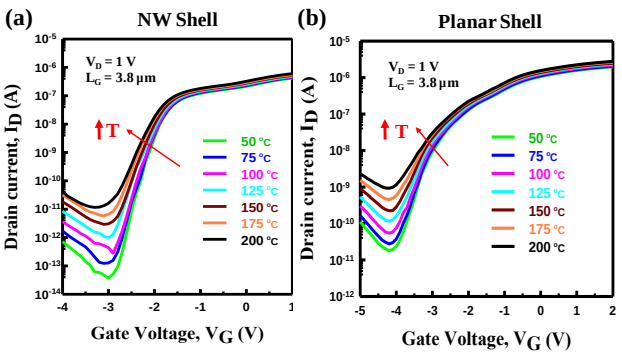

Fig. 7. Temperature dependence (50°C to 200°C) on I_D-V_G characteristics of the (a) NW shell JL-FET and (b) planar shell JL-FET.