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Ambipolar operation of asymmetric Ge Schottky tunneling source field-effect transistor fabricated on Ge-on-Insulator

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Abstract

Asymmetric Schottky tunneling source (STS) FET was fabricated on Ge-on-Insulator (GOI) substrate. GOI was made by using Smart-Cut™ technique. Fabricated STS FET with PtGe and TiN electrodes well operated as both n- and p-FETs, which means carrier injection was succeeded in both PtGe/Ge and TiN/Ge interfaces.

1. Introduction

Asymmetric Schottky tunneling source (STS) FET is an alternative device structure to overcome problems related advanced scaling. Its operation principle is carrier injection by field emission (FE) to the channel under strong accumulation or inversion condition induced by gate voltage (V_G), as shown in Fig. 1 [1-4]. Ideally, this device structure can completely suppress short channel effect because of no depletion layer in channel/drain junction. Furthermore, it can be apply to steep slope tunneling FET by addition of heavily doped (n^+ or p^+) source pockets [5,6].

We have reported Ge STS FET with PtGe and TiN source/drain fabricated on bulk Ge substrate [7]. PtGe and TiN have high electron and hole barrier heights for Ge, respectively. The device well operated as n-FET, which means that electron is successfully injected from PtGe source to accumulated channel. However, p-FET operation has not succeeded. In addition, it is necessary to introduce Ge-on-Insulator (GOI) substrate for performance improvement.

In this study, we fabricated Ge asymmetric STS FET on GOI substrate. GOI was fabricated by using wafer bonding and layer splitting methods which are well known as Smart-Cut™ [8]. Fabricated device successfully shows ambipolar operation as both n- and p-FETs.

2. Experimental

Sample fabrication procedure is shown in Fig. 2. In this study, we prepared (100) n-Ge with N_D of 1.7×10^{17} cm^{-3} and (100) n-Si with N_D of 7×10^{14} cm^{-3} as donor and handle substrates, respectively. After H^+ implantation through 100 nm-thick SiO_2 and subsequent SiO_2 removal, 3 nm-thick ALD-Al_2O_3 was deposited on Ge substrate. On the other hand, 120 nm-thick thermally grown SiO_2 was formed on Si substrate. Ge and Si were manually bonded in cleanroom environment. Layer splitting was carried out by annealing at 400°C. In order to remove defective layer, Ge was thinned by wet etching used dilute H_2O_2 solution. Then chemical mechanical polishing (CMP) was performed to make flat surface. For electrical property improvement, the sample was annealed at 500°C for 1h in N_2 ambient [8]. Then, Ge isolation was performed to island shape for device region by H_2O_2 wet etching. Device fabrication procedure is almost the same as our previous work [7]. Pt and TiN electrodes were deposited and patterned using sputtering and liftoff techniques. After post metallization annealing (PMA) at 400°C, $Al_2O_3/SiO_2/GeO_2$ gate insulator was formed using combination of sputtering and ALD. After postdeposition annealing (PDA) at 400°C, TiN gate electrode was formed using sputtering. Finally, contact holes for S/D were opened and contact Al pads were made by resistive evaporation.

3. Result and Discussion

Figure 3(a) shows an AFM image of the GOI surface after isolation. CMP effectively improves surface flatness of the GOI. Figure 3(b) shows a side wall of the isolated Ge island. Wet etching by H_2O_2 made taper shape side wall. This may be caused Ge isotropic etching by H_2O_2.

Output characteristic (I_D-V_D) and transfer characteristic (I_D-V_G) of the fabricated device are shown in Fig. 4(a) and 4(b), respectively. Here, circuit connection and applied voltage are set for n-FET operation, as shown in Fig. 4(c). It showed typical n-FET operation, which is the same with our previous study on bulk Ge substrate [7]. Positive V_G induces electron accumulation layer in the GOI island and current conduction mechanism at on-state may be estimated as FE tunneling between PtGe and GOI channel (Fig. 4(c)). However, large off and small on current must be improved.

Figures 5(a) and 5(b) are I_D-V_D and I_D-V_G characteristics under p-FET circuit connection, which is also shown in Fig. 5(c). Similar to Fig. 4, normal p-FET operation was observed. Negative V_G makes hole inversion channel in the GOI. Therefore, possible current conduction mechanism is FE tunneling between TiN and GOI inversion channel (Fig. 5(c)). We had not observed p-FET operation in our previous work on bulk Ge [7]. Difference between the previous and this studies is interfacial structure of TiN/Ge contact. Planer interface in previous study prevents efficient carrier transport, as shown in Fig. 6. On the other hand, taper shape TiN/Ge interface under gate stack supports carrier transport. Therefore, GOI and taper shape metal-channel interface is suitable to realize STS p-FET.

4. Conclusions

We fabricated asymmetric STS FET on GOI substrate. Fabricated device successfully operated as both n- and p-FETs. Taper shape GOI side wall may support efficient carrier injection between TiN and inverted channel.

Acknowledgements

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References

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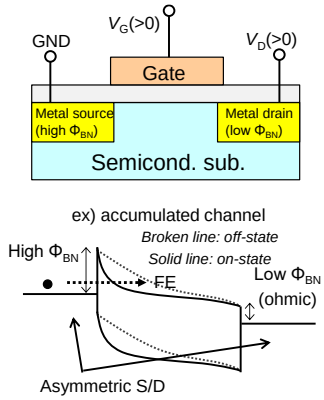
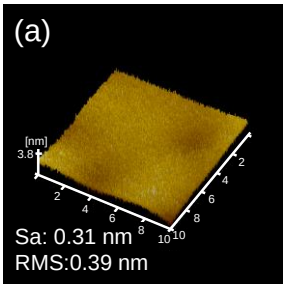


Fig. 1 Cross sectional image of STS FET and band diagram under off-state (broken line) and on-state (solid-line).



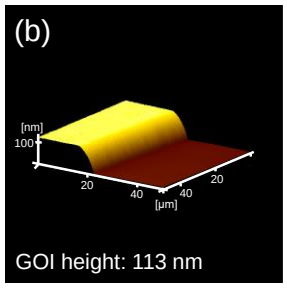


Fig. 3 AFM images of the GOI. (a) surface roughness and (b) side wall of the isolated GOI island.

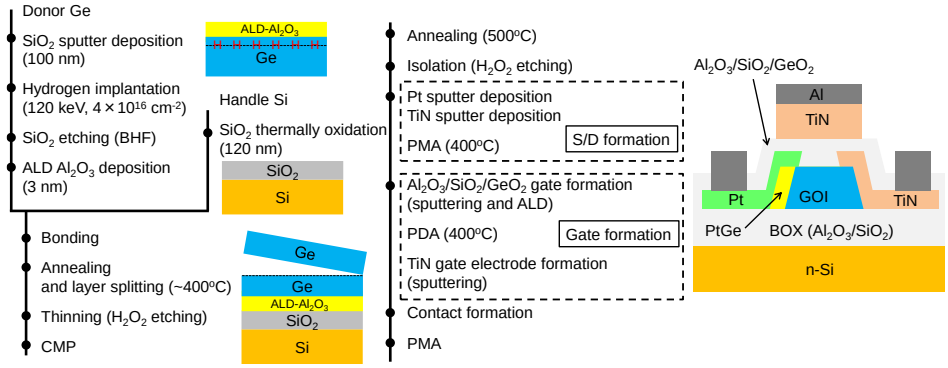


Fig. 2 Sample fabrication procedure and cross sectional image of fabricated STS FET on GOI.

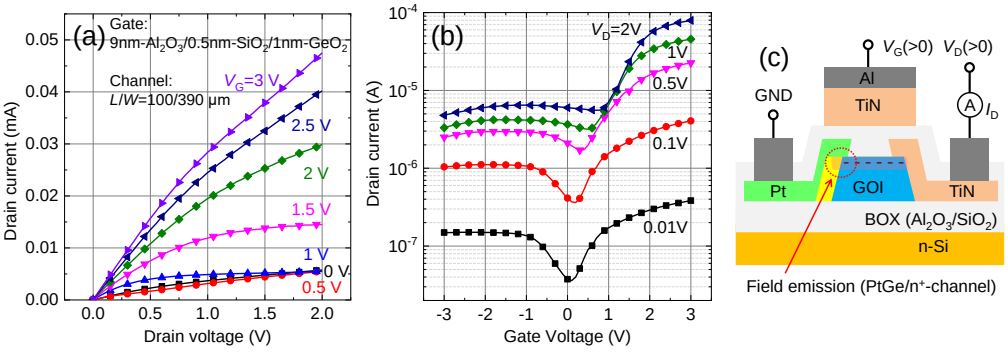


Fig. 4 (a) I_D-V_D, (b) I_D-V_G characteristics under n-FET operation. Circuit connection and applied voltages are also shown in (c).

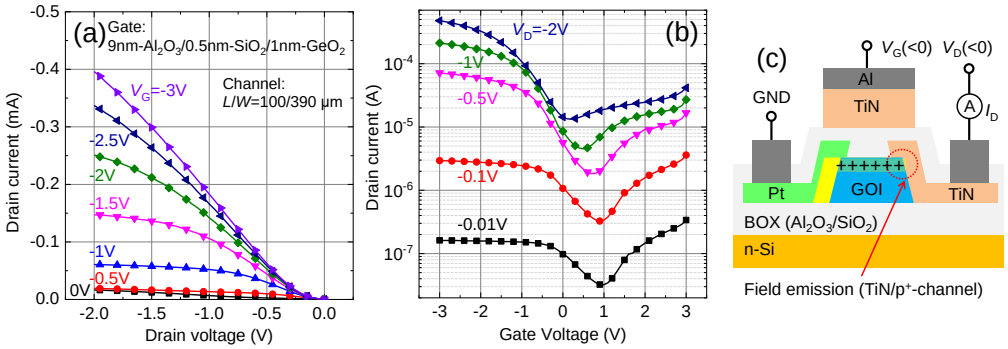


Fig. 5 (a) I_D-V_D, (b) I_D-V_G characteristics under p-FET operation. Circuit connection and applied voltages are also shown in (c).

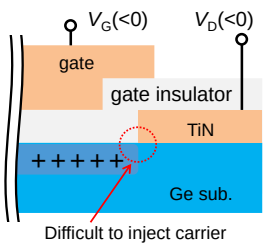


Fig. 6 Schematic image of TiN/Ge interface for STS FET fabricated on bulk Ge in our previous work [7]. Planer shape junction seems hard to inject carrier.