Extended Abstracts of the 2018 International Conference on Solid State Devices and Materials, Tokyo, 2018, pp851-852

Improvement in GaAsSb/InGaAs double-gate tunnel FET using thermal evaporation for gate electrode and Al_2O_3/ZrO_2 for gate insulator

Ryosuke Aonuma[1], Nobukazu Kise[1] and Yasuyuki Miyamoto[1]

[1] Department of Electrical and Electronic Engineering, Tokyo Institute of Technology
2-12-1-S9-2, O-okayama, Meguro-ku, Tokyo 152-8552, Japan
Phone: +81-3-5734-2572 E-mail: miya@pe.titech.ac.jp

Abstract

We fabricated double-gate vertical GaAsSb/InGaAs tunnel FETs. The characteristic of these tunnel FETs were improved by changing the gate electrode evaporation from electron beam to thermal evaporation. Furthermore, by changing the insulator from Al_2O_3/HfO_2 to Al_2O_3/ZrO_2, the steepest subthreshold slope (SS_{MIN}) = 56 mV/dec at V_{DS} = 0.2 V was achieved.

1. Introduction

Tunnel FETs (TFETs) can achieve steeper subthreshold slopes (SSs) using the tunneling effect and are promising as elements for the next-generation low-power-consumption circuits [1]. We simulated high-performance TFETs with a double-gate structure using GaAsSb/InGaAs [2] and reported an experimental approach [3].

The problem in the SS improvement of TFETs is the reduction in the interface state density (D_{it}). D_{it} causes leakage current, reduces gate controllability, and degrades the SS. The gate electrode formation process greatly influences the D_{it} [4]. The increase in the insulator capacitance using Al_2O_3/ZrO_2, which is a high dielectric constant material, can provide the reduction in D_{it} [5].

In this study, we report the improvement in SS of TFETs using thermal evaporation and an Al_2O_3/ZrO_2 insulator.

2. Device fabrication

The characteristic improvement by changing from electron beam to thermal evaporation is performed by TFETs with Al_2O_3-1nm/HfO_2-3.5nm (1.1 nm as EOT) as the insulator. Subsequently, TFETs with Al_2O_3-1nm/ZrO_2-3.5nm (0.9 nm as EOT) as insulator were fabricated with gate electrode formed by thermal evaporation.

The fabrication processes are almost similar to our former reports [3]. The epitaxial structure for the devices consists of p^{++}-GaAsSb (8×10^{19} cm^{-3}) / i-InGaAs / n^{++}-InGaAs (8×10^{18} cm^{-3}). Initially, by using a TiW drain electrode formed as a mask, an InGaAs layer was etched using ICP-RIE. Successive undercut etching of an InGaAs channel layer reduced the InGaAs body width. An insulator was deposited at 300 °C using atomic layer deposition. After the insulator etching at the top of the drain electrode, Ni gate electrodes were evaporated by an oblique deposition at 45°. After the BCB coating and etchback, contact holes were opened. Finally, electrode pads were formed, as shown in Fig.1 schematically. The TEM image of the fabricated TFET is shown in Fig. 2. A sub-10-nm-wide body is confirmed.

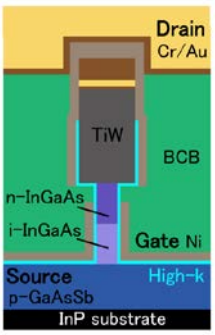

Fig.1 Schematic of double-gate tunnel FET.

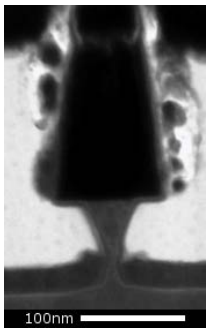

Fig.2 TEM image of fabricated tunnel FET.

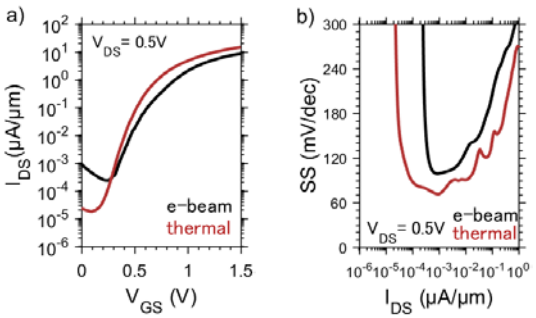

Fig.3 Electrical characteristics of TFET with gate electrode deposited by electron beam evaporation and thermal evaporation. a) I_{DS}–V_{GS} and b) SS–I_{DS}. Gate insulator was an Al_2O_3/HfO_2 layer.

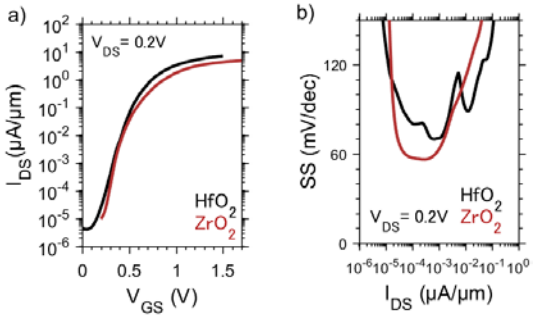

Fig.4 Electrical characteristics of TFETs with Al_2O_3/HfO_2 and Al_2O_3/ZrO_2 using thermal evaporated gate electrode. a) I_{DS}–V_{GS} and b) SS–I_{DS}.

3. Device measurement at room temperature

Changes in the I_{DS}–V_{GS} and SS–I_{DS} characteristics by evaporation when the gate insulator was Al_2O_3/HfO_2 are as shown in Fig. 3. In the thermal evaporation, the off current was smaller

by one order of magnitude, and the SS improved in the entire subthreshold region. Changes in the I_{DS}–V_{GS} and SS–I_{DS} characteristics between Al_2O_3/HfO_2 and Al_2O_3/ZrO_2 are shown in Fig. 4. A gate metal was deposited by thermal evaporation. In the case of Al_2O_3/ZrO_2, the rise in I_{DS} became steeper and the SS improved. The SS_{MIN} was 56 mV/dec and the SS_{ave} (SS averaged over three digits) improved from 86 mV/dec to 74 mV/dec at V_{DS} = 0.2 V, and the on/off ratio was 6×10^5 at V_{DS} = 0.5 V.

4. Low-temperature measurement

To confirm that the primary component of the current is band-to-band tunneling, low-temperature measurements were performed, as shown in Fig. 5. The temperature range was from 150 K to 250 K with V_{DS} = 0.5 V. The SS_{MIN} was 47 mV/dec at 150 K with the combination of thermal evaporation and Al_2O_3/ZrO_2. As a reference, the results by combining E-beam evaporation and Al_2O_3/HfO_2 is also shown. The temperature dependence is clearly weak in the combination of thermal evaporation and Al_2O_3/ZrO_2.The temperature dependence was evaluated by two methods, i.e., trap -assisted tunneling (TAT)[6] and tunneling through band tail[7].

For TAT, we used an Arrhenius plot as shown in Fig. 6 and extracted the gate bias dependence of the activation energy (E_A), as shown in Fig. 7. When V_{GS} is large, the estimated E_A decreases, because the current is dominated by band-to-band tunneling. As the E_A decreases because of the change in the gate electrode evaporation, we confirmed that the TAT is reduced.

Next, we evaluated the band tails. At first, the energy attenuation parameter E_0 from the NDR characteristic was extracted [6]. As NDR characteristics were not observed in TFETs with E-beam evaporation, TFETs using thermal evaporation were evaluated for the band tail. Fig. 8 shows the E_0 obtained from the slope of the NDR characteristic. The reduction in E_0 by the gate insulator was observed, as shown in Fig. 8. The calculated SS was 35 mV/dec at room temperature using E_0 = 38 mV when D_{it} is zero. However, as shown in Fig.8, E_0 changes with the change in the gate structure even though both devices were fabricated from the same substrate. Moreover, E_0 was changed from 113 meV at 300 K to 38 meV at 50 K. Thus, the observed E_0 cannot be explained by the simple band tail of the bulk. Further studies are required for an accurate analysis.

5. Conclusions

In the GaAsSb/InGaAs double-gate TFETs, we investigated the influence of using thermal evaporation for gate electrode formation and using Al_2O_3/ZrO_2 for the insulator. We achieved SS_{MIN} = 56 mV/dec with TFETs using Al_2O_3/ZrO_2 and thermal evaporation. We also examined the deterioration factors of SS and evaluated the TAT and band tail as a temperature-dependent leak component.

Acknowledgements

Fig. 2 was aided by the Okayama analysis department of the Tokyo Institute of Technology.

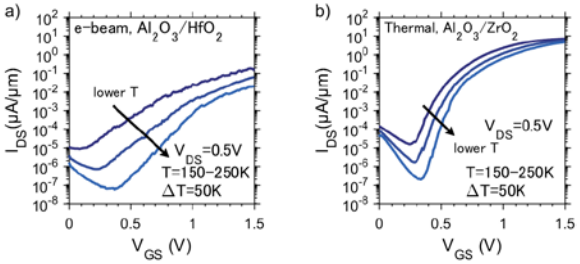

Fig.5 I_{DS}–V_{GS} characteristics at low temperature. a) E-beam evaporation and Al_2O_3/HfO_2. b) Thermal evaporation and Al_2O_3/ZrO_2.

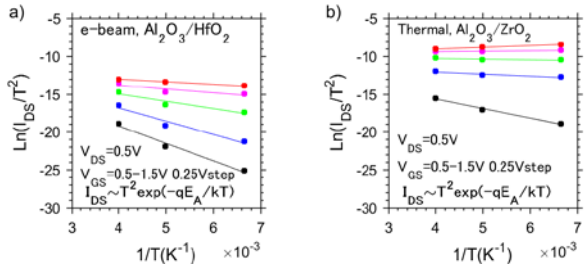

Fig.6 The Arrhenius plot for a) E-beam evaporation and Al_2O_3/HfO_2 and b) thermal evaporation and Al_2O_3/ZrO_2..

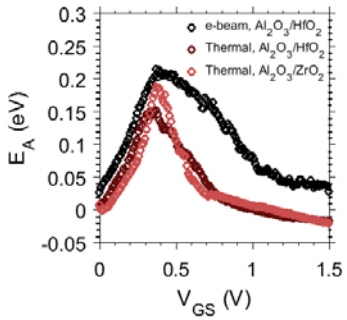

Fig.7 E_A–V_{GS} characteristics with change in evaporation and insulator.

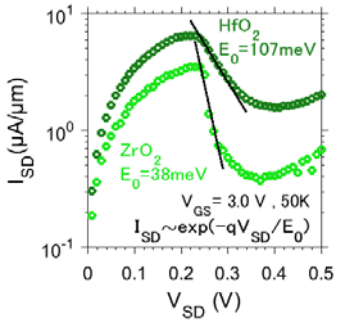

Fig.8 I–V characteristics with differentiated negative resistance.

References

[1] A. M. Ionescu, et al., Nature 479, 329 (2011).
[2] S. Iwata, et al., IEEJ Trans. EIS 136, 4, p.467 (2016).
[3] M. Fujimatsu, et al., IPRM 2012, Mo-1D.2. and N. Kise, et al., CSW 2017, C804.
[4] G. J. Burek, et al., J. Vac. Sci. Technol. B 29, 040603 (2011).
[5] J. Huang, et al., IEEE IEDM, dec 2009, p.1 (2009)
[6] S. Mookerjea, et al., IEEE EDL, 31, 6, p.564, (2010).
[7] E. Memisevic, et al., IEEE EDL, 38, 12, p.1661, (2017).