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Significant Improvement in Electrical Characteristics of FinFETs by Trilayer High-k Gate Dielectric

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Abstract

Although the stacked high-k gate dielectric was proposed to reduce EOT in MOSFETs, its applications on FinFETs are rarely seen. A higher drive current, a higher on/off current ratio, a smaller S.S. value, a lower gate leakage current, a higher peak electron mobility, and better reliability characteristics of FinFETs are simultaneously achieved by a Zr-rich trilayer gate dielectric. The improvement can be attributed to fewer oxide traps in gate dielectric.

1 Introduction

With evolution of Moore's law, high-K/metal gate (HK/MG) and FinFET technologies have become mainstreams for ultimately scaled CMOS devices at and beyond the 16 nm technology node [1]. However, gate oxide scaling has been leaded towards a limitation for Hf-based HK dielectrics [2]. Many approaches have been proposed to further follow the device scaling trend, like new HK material [3], gate all around (GAA) structure [4]. ZrO_2 has a similar bandgap and band-offset [5] and even higher dielectric constant [6] as compared to HfO_2. However, ZrO_2 with relatively insufficient thermal stability may lead to chemical reactions with channel region, which may induce a large amount of interface defects [7]. Besides, the interface between metal gate and high-k dielectric is also very important to device characteristics, because oxygen vacancy generation in high-k dielectrics may induce threshold voltage shifts and some reliability problems [8]. Therefore, a novel trilayer HK dielectric gate stack is proposed for FinFET in this work. Electrical characteristics and reliability of FinFETs with control (HfO_2), bilayer (ZrO_2/HfO_2), Hf-rich and Zr-rich trilayer ($HfO_2/ZrO_2/HfO_2$) gate stacks are investigated and compared.

2 Experiments

FinFETs were fabricated on 6-inch p-type SOI (100) wafers. The patterns of dummy fins were defined by I-line lithography. Reactive ion etching (RIE) process was performed to form four parallel fins with a fin height of 30 nm. Then, a trimming was performed on the fins with H_2 plasma for 300 s. Afterwards, the SiO_2 IL was formed in H_2O_2 solution at 75 °C for 10 min. Then, a 3 nm thick HfO_2 (control), a 1.5 nm/1.5 nm thick ZrO_2/HfO_2 (bilayer), a 1.0 nm/1.0 nm/1.0 nm thick $HfO_2/ZrO_2/HfO_2$ (Hf-rich trilayer) and a 0.5 nm/2.0 nm/0.5 nm thick $HfO_2/ZrO_2/HfO_2$ (Zr-rich trilayer) were deposited by an atomic layer deposition (ALD). Afterward, a 100-nm thick TiN film was deposited by sputtering to serve as metal gate. After patterning gate stack, phosphorous implantation (at 40 keV for a dose of 5×10^{15} cm^{-2}) and activation (750 °C for 30 s) were performed on all samples. Passivation and metallization processes were performed, followed by a sintering at 400 °C for 30 min to complete the device fabrication. The sample splits are shown in Table 1.

3 Results and Discussion

Fig. 1 shows transmission electron microscopy (TEM) images of FinFET structure. The height and width of fin channel are about 30 nm and 13 nm, respectively. The thickness of gate dielectric is ~3.0 nm for all samples, which can also be seen from the TEM image.

Table. 1: Sample splits of FinFETs in this work

Sample	Control	Bilayer	Hf-Rich Trilayer	Zr-Rich Trilayer
Sinter	400 °C 30 min			
Contact	Al-Si-Cu 200nm			
Activation	RTA 750°C 30s			
Metal gate	TiN 100nm			
High-k	HfO_2 30Å	HfO_2+ZrO_2 15Å 15Å	HfO_2+ZrO_2+HfO_2 10Å 10Å 10Å	HfO_2+ZrO_2+HfO_2 5Å 20Å 5Å
Trimming	300s H_2			
Channel material	Single Crystal-Si			
Substrate	SOI			

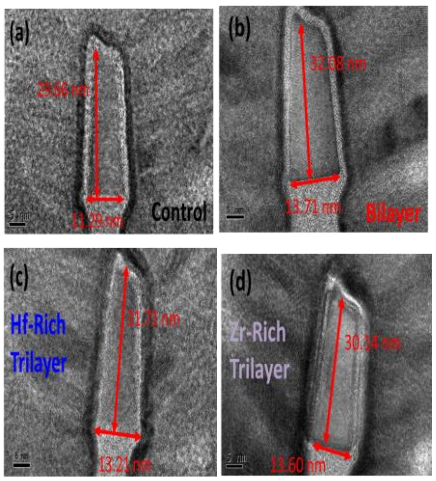

Fig.1: TEM images of FinFETs with (a) control, (b) bilayer, (c) Hf-rich trilayer and (d) Zr-rich trilayer gate stacks in this work.

Fig. 2 shows (a) drain current versus gate voltage (I_d-V_g) and (b) drain current versus drain voltage (I_d-V_d) of FinFETs with control, bilayer, Hf-rich trilayer and Zr-rich trilayer gate stacks, respectively. The on/off current ratio of FinFET is improved to 2.2×10^8 by using Zr-rich trilayer gate stack. The sub-threshold swing (S.S.) values of samples with Zr-rich trilayer, Hf-rich trilayer, bilayer, and control one are 69, 71, 70, and 72 mV/dec, respectively. The S.S. value of sample with Zr-rich trilayer gate dielectric is relatively smaller, probably due to fewer oxide traps in gate dielectric. The drive current of sample with Zr-rich trilayer gate dielectric is increased about 200% as compared to that of control one, as shown in Fig.2 (b). Results indicate that sample with Zr-rich trilayer gate stack shows better gate control ability and lower interface traps.

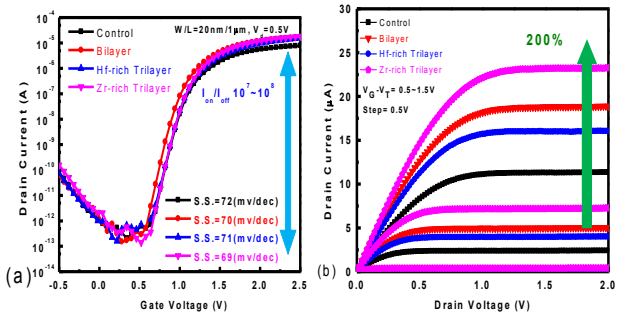

Fig. 2 (a) I_d-V_g curves and 2 (b) I_d-V_d curves for FinFETs with control, bilayer, Hf-rich trilayer and Zr-rich trilayer gate stacks.

Fig. 3 shows (a) gate leakage current versus gate voltage (J_g-V_g) curves and (b) electron mobility (μ_{eff}) versus inversion charge density (N_{inv}) for FinFETs with control, bilayer, Hf-rich trilayer and Zr-rich trilayer gate stacks. The gate leakage current of device with Zr-rich trilayer gate stack is much lower than those with the others. The peak electron mobility values of samples with Zr-rich trilayer, Hf-rich rilayer, bilayer, and control gate dielectrics are 345, 270, 340, and 274 cm^2/Vs, respectively. A 22% enhancement of peak electron mobility can be achieved by using a Zr-rich trilayer, which may be due to fewer oxide traps in gate dielectric obtained from a higher content of ZrO_2.

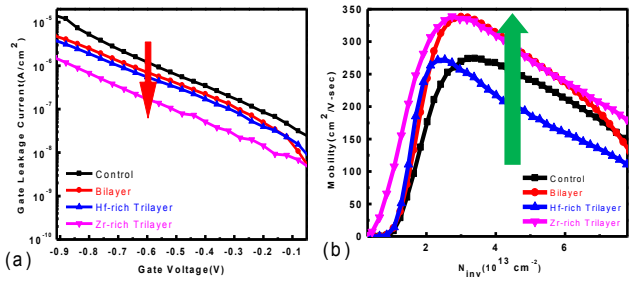

Fig. 3 (a) J_g-V_g curves and (b) electron mobility (μ_{eff}) versus N_{inv} for FinFETs with control, bilayer, Hf-rich trilayer and Zr-rich trilayer gate stacks.

Fig. 4 shows (a) threshold voltage shift ($V_{th\text{-}shift}$) and (b) degradation of maximum trans-conductance ($G_{m,max}$) versus stress time at a constant voltage stress (E=9 MV/cm) for FinFETs with control, bilayer, Hf-rich trilayer and Zr-rich trilayer gate stacks. The stress-induced $V_{th\text{-}shift}$ value of sample with Zr-rich trilayer gate dielectric is much smaller than that of control one. Results indicate that a ZrO_2 dielectric in trilayer high-k dielectrics can suppress oxygen vacancy generation in gate stack. In addition, sample with trilayer high-k dielectric gate stack show lower threshold voltage shifts, suggesting that the interface quality between gate electrode and high-k dielectric can be clearly improved by the proposed trilayer high-k dielectric stack. The stress-induced degradation of $G_{m,max}$ for all samples is similar, indicating that the inter-diffusion between ZrO_2 layer and channel region can be suppressed by inserting a HfO_2 layer.

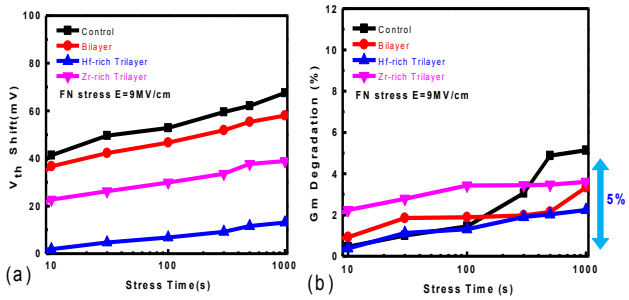

Fig. 4 (a) $V_{th\text{-}shift}$ and (b) $G_{m\text{-}max}$ degradation versus F-N stress time of FinFETs with control, bilayer, Hf-rich trilayer, and Zr-rich trilayer gate stacks.

4 Conclusions

FinFETs with HfO_2, ZrO_2/HfO_2 bilayer, Hf-rich trilayer and Zr-rich trilayer gate stacks are investigated and compared in this work. A higher drive current, on/off current ratio, peak electron mobility, a lower S.S. value, gate leakage current, and better reliability characteristics of FinFETs are achieved by using Zr-rich trilayer gate stack. Therefore, a Zr-rich trilayer dielectric gate stack is promising to achieve high performance HK/MG FinFETs.

Acknowledgment

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References

[1] Chenming Hu et al., IEEE Trans. Electron Devices. 47 (2000), pp. 2320-2325.

[2] Chen-Chien Li, Kuei-Shu Chang-Liao et al., IEEE Electron Device Lett. 37 (2016), pp. 12-15.

[3] D. H. Triyoso et al., IEEE Electron Device Lett. 29 (2008), pp. 57–59.

[4] N. Singh et al., IEEE Electron Device Lett. 27 (2006), pp. 383–386.

[5] V. V. Afanas'ev et al., Appl. Phys. Lett. 99 (2011), pp. 172101-1–172101-3.

[6] D. Fischer and A. Kersch, Appl. Phys. Lett. 92 (2008), pp. 012908-1–012908-3.

[7] M. Gutowski et al., Appl. Phys. Lett. 80 (2002), pp. 1897–1899.

[8] K. Shiraishi et al., International Conference on Solid-State and Integrated-Circuit Technology, (2008), pp. 1256–1259.