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Vertical gate-all-around transistors with symmetrical silicided S/D contacts for high performance p-FET devices.

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Abstract

Vertical gate-all-around nanowire (NW) FET has been identified as a promising candidate to pursue the device miniaturization below 5nm TN. Here, a large-scale processing of GAA vertical silicon nanowire MOSFETs is presented with a particular emphasis on the formation of low resistive silicided nanocontacts. Promising overall electrical performances were obtained, with excellent electrostatic behavior and high drive current for 14-nm gate length p-FETs.

1. Introduction

Gate - all - around nanowire (NW) FET are a natural extension of current FinFET architectures, where the gate is totally wrapped around the conduction channel of the transistors, leading to a strong reinforcement of the electrostatic control of the carriers moving through the channel. This architecture can be performed with two flavors: planar (lateral) [1] or vertical configurations [2]. The lateral configuration still uses conventional 2D layouts and is facing the same physical limits as those of FinFET, for instance the space for the contact area or the congestion of the metallic lines in the interconnection levels. It is possible to perform a 3D stacking of these lateral transistors but we are reaching the technological limits of this approach. Vertical GAA NW FET, a more disruptive technology, allows moving from 2D to a truly 3D layout configuration, with the gate length of the transistor defined vertically. Vertical integration is a particularly attractive approach because of its intrinsic 3D nature, which is more favorable to scale the contacted gate pitch i.e. scaling of the gate length and contact area [3]. The vertical NW transistor is much easier to manufacture, because the gate length is simply defined by the thickness of the deposited gate material [2].

However, this real 3D architecture is faced to challenges in term of material and processing issues. Indeed, very recent demonstration of VFETs [4] [5] [6] illustrated the same device limitations (difficulty in gate-all -around engineering that prohibits a device scaling, absence of identical S/D contacts with bottom contacts taken directly on the bulk semiconductor). Moreover, all these demonstrations focused on nFET polarity, and very few demonstrations are related to the complementary polarity (pFETs). Here, we present the demonstration of scaled and symmetrical devices based on vertical silicon nanowires with gate all around and silicided source / drain. Excellent static performances on pFET are obtained in term of electrostatic control (short channel effect limitations) and drive current.

2. 3D device fabrication

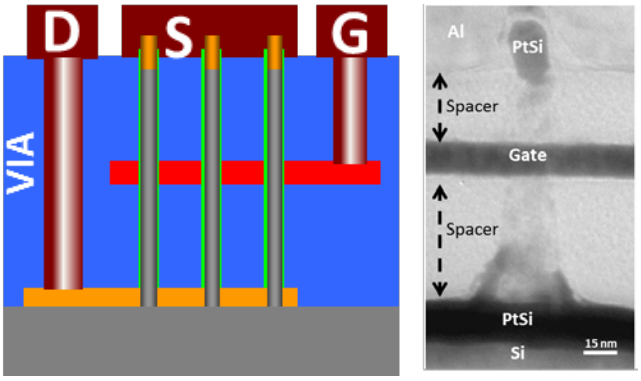

Fig. 1 Schematic view of a vertical FET device implemented on a dense nanowire array with extrinsic access connecting different levels and TEM cross section of the device with a gate all around the nanowire and symmetrical silicided S/D (PtSi) contacts.

The main step of process fabrication of such a vertical FET device is as followed: (1) The formation of highly doped wells (with n-type or p-type) with a flat doping profile (~ 10^{19} at/cm3) where (2) NW arrays of each transistor are fabricated by electron beam lithography patterning of circular nanopillars subsequently transferred in the Si substrate by RIE. Then, using the stress retarded oxidation phenomenon, Si NWs are shrunk and the formed oxide is stripped (3) A 5-nm-thick gate dioxide is grown by dry oxidation at 725°C and an anisotropic RIE etching step is performed to remove the oxide layer at the top and bottom of the NWs without altering the gate oxide

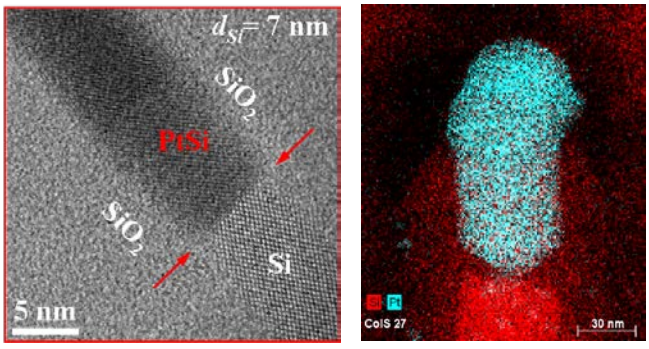

Fig. 2: HR TEM cross section coupled with EDX analysis of PtSi

nanocontact on Si NW.

(4). A 15-nm-thick platinum (Pt) layer is anisotropically deposited to cover the top and the bottom of NWs and the silicidation is activated by RTA at 500°C/ 3 min for forming the metallic (PtSi) S/D contacts. This step has been intensely studied in order to master the formation of 3D nanocontacts based on systematical high resolution TEM cross section coupled with EDX analysis (as illustrated in Fig.2). The kinetics of reaction, the phase formation with diameter dependence has been demonstrated and optimized process proposed to get low resistive metallic contacts with a controlled morphology. (5). Then, another key step of the process has been developed in order to perfectly mastering of the insulating layer between the contact electrodes (source, gate, drain) to achieve symmetrical and ultra-scaled devices. An approach combining spin on glass (SOG) planarization, where the NW network is embedded in the dielectric matrix and a chemical etch back in highly diluted HF solution is used to control the dielectric top layer at the nanoscale. Then, (6) a 15-nm-thick metal layer (Cr or Ni) is anisotropically deposited to form the surrounded gate in the middle part of Si NWs. (7) A second spacer is etched back down to the top part of the NWs (PtSi terminations). Two via-holes through the dielectric layer to connect the bottom contact (PtSi layer) and the gate contact (Cr layer). (8) Finally, a 400-nm thick aluminum layer is patterned to form the contact pads. Fig. 1 right is a TEM cross section of the final device that integrates parallel dense silicon NW arrays with symmetrically silicided S/D and scaled metallic GAA (L_g ~ 14 nm) architectures.

3. Electrical performance

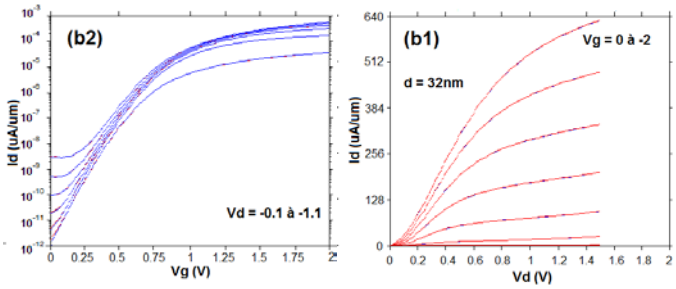

Fig. 3: Transfer characteristics of 14 nm GAA p-MOSFET on Si VNW with a diameter of 32 nm.

An example of static characteristics is presented in Fig. 3 on a transistor with Lg= 14nm and NW diameter of 32nm. The p-type device exhibits normally off behavior with high control over short channel effects with almost-ideal subthreshold characteristics (SS = 95 mV/dec and DIBL = 38 mV/V) and I_{on}/I_{off} ratio up to 5 decades. A drive current of 490µA/µm is obtained at V_d=- 0.8V, which is the best performance published for a p-type VFET, in line with the ITRS projection [7] for the low power 5nm technology node. The optimization of access resistance, in particular based on the detailed study of silicided nanocontacts on NW, is of prime importance, leading to a Rext ≈ 200 Ohm.µm.
The device operates in accumulation regime (junctionless mode). When the transistor is turned on, the channel conduction is made by the entire section of the NW whereas when it turned off, the gate field can deplete the entire volume of the NW. Nevertheless, when the NW is too large, the channel is only partially depleted. The immunity against short channel effect becomes weak leading to a poor control of the device with large increase of off current. Fig.4 shows these evolutions with the variation of SS (Fig. 4left) and Ion/Ioff ratio (Fig.4 right) as a function of NW diameter.

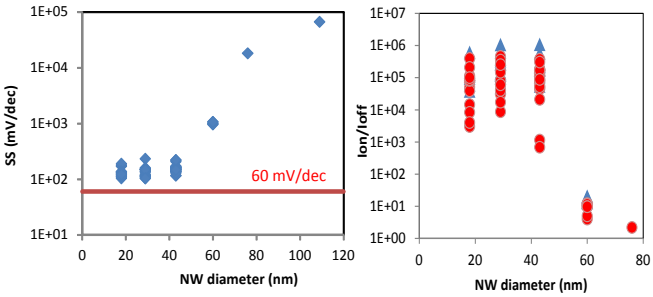

Fig. 4: SS and Ion/Ioff ratio as a function of NW diameters

4. Conclusions

We presented symmetrical vertical devices implemented on silicon nanowires with nanometric scale gate-all-around and silicided source / drain contacts. Excellent static performances in term of electrostatic control and drive current have been demonstrated on pFET.

Acknowledgements

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