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Steep Switching Less Than 15 mV/decade in Silicon-on-Insulator Tunnel FETs by Trimmed-Gate Structure

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We propose a novel trimmed-gate (TG) structure, which substantially decreases the subthreshold swing (*SS*) of tunnel field-effect transistor (TFET). Our Technology computer-aided (TCAD) simulations demonstrate that the TG structure strongly suppresses the off leak component of band-to-band tunneling (BTBT) current. As a result, extremely steep *SS* less than 15 mV/decade can be realized in a silicon-on-insulator (SOI) TFET. We also demonstrate that the *SS* improvement thanks to the TG structure is enhanced by a high source doping.

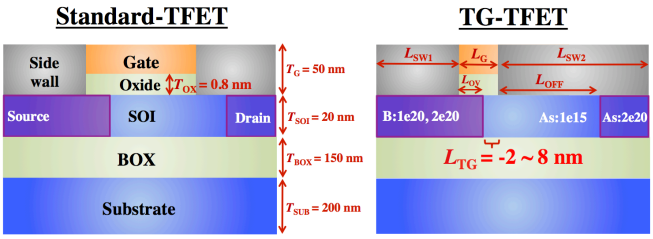
1. Introduction

TFET is one of steep slope transistors that achieve steep *SS* less than 60 mV/decade which is the physical limit of MOSFETs at 300K [1]. Therefore, TFET has attracted much attention as building blocks for low-power LSIs in next generation [2]. However, unlike a conventional MOSFET, the *SS* of TFET increases with a gate voltage. Thus, the "average" *SS* degrades as the operation voltage increases. Hence, various technologies have been investigated to realize a better average *SS*. In particular, isoelectronic trap technology [3,4] and channel material engineering with Ge or III-V materials [5,6] have succeeded in improving the average *SS* by increasing I_{ON}. On the other hand, these technologies do not contribute to the reduction of the off leak component of the current, which is another key to improving the average *SS*.

In this work, we investigate steep switching in TFETs having a trimmed-gate (TG) structure, which realizes steep *SS* by reducing off leak component of BTBT current. In addition to our recent work on double-gated TFETs [7], we numerically demonstrate that SOI TFETs with TG structure can achieve average *SS* less than 15 mV/decade. We also show that a high source doping is preferable for steeper switching with the TG structure.

2. Model and Method

Figure 1 indicates a schematic representation of the TFET w/o the TG structure (Standard-TFET) and w/ the TG structure (TG-TFET). In the TG-TFET, the gate is trimmed to near the source edge, because of which the channel region in which the gate electrostatic control is effective becomes extremely short. To discuss the effect of *SS* improvement by the TG structure, we performed 2D device simulations for the both TFETs by using drift-diffusion-based TCAD simulator HyENEXSS [8-10]. The dimensions and the dopant concentrations of the TFETs are shown in Fig. 1. In this work, an abrupt doping profile is assumed. We employed non-local BTBT model with the BTBT generation rate given



Length (nm)	L_{OV}	L_G	L_{OFF}	L_{SW1}	L_{SW2}
Standard- TFET	10	40	40	60	60
TG-TFET	10	8~18	62~72	60	82~92

Fig. 1. Schematic figure of the TFETs w/o the TG-structure (Standard-TFET) and w/ the TG-structure (TG-TFET).

by $G_{BTBT} = A(E_{NL}/E_0)\,\gamma \exp(-B/E_{NL})$, where the E_{NL} is the non-local electric field, and the constant E_0 =1V/cm. As for the physical parameters, we chose $A = 2.4\times10^{15}$ cm^{-3} s^{-1}, B = 1.9 MV/cm, and γ = 2.5, which are typical values for BTBT at silicon PN junctions.

3. Results

Firstly, we start with the characteristics of standard-TFET with the source doping concentration $N_{source} = 2\times10^{20}$ cm^{-3}. Figure 2(a) shows the drain current I_D as a function of gate-source voltage V_{GS} at a drain voltage V_D = 0.3 V. Figures 2(b) and 2(c) indicate the distributions of BTBT generation rate near the source edge in the standard-TFET for V_{GS} = 0.6 V and 1.8 V, respectively. The magenta lines correspond to the contours of electrostatic potentials $\Psi = \Psi_{hmax}$ and $\Psi = \Psi_{hmax} + E_G$. Here, Ψ_{hmax} is the potential energy at which the generation rate of the hole originating from BTBT is maximized, and E_G is the energy gap of silicon. As shown in Fig. 2(b) and 2(c), the strong carrier tunneling takes place between the contour lines, and the length of the major tunneling path becomes short with the increase in V_{GS}. In the Standard-TFET, the increase of I_D is derived from the continuous decrease of the tunneling length.

Then, we discuss the switching characteristics of the TG-TFETs by varying the trimmed-gate length, $L_{TG} = L_G - L_{OV}$, which gives the distance between the gate and source edge. Figure 3(a) shows I_D versus V_{GS} curves for the TG-TFETs with $N_{source} = 2\times10^{20}$ cm^{-3} and L_{TG} = -0.5-4 nm. The dotted line indicates the I_D-V_{GS} curve for the Standard-TFET as a reference. In comparison with the Standard-TFET, the switching slopes of the TG-TFETs are significantly improved without the reduction in I_D under a high V_{GS}. The distributions of the BTBT generation rate in the TG-TFET with L_{TG} = 2 nm for V_{GS} = 0.6 V and 1.8V are shown in Figs. 3(b) and 3(c). It is quite remarkable that BTBTs completely disappear in the TG-TFET when V_{GS} is

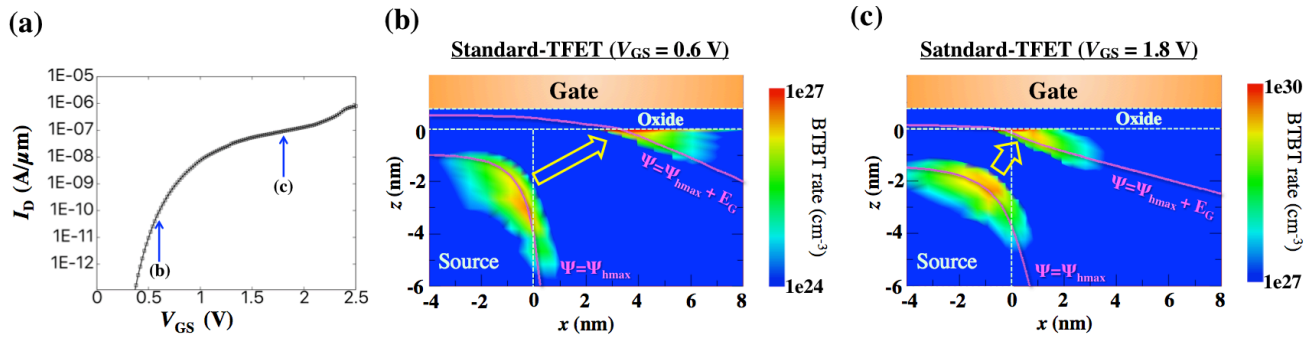


Fig. 2. (a) I_D as a function of V_{GS} for the Standard-TFET. (b), (c) The distribution of the BTBT generation rate near the source in the Standard-TFET for V_{GS} = 0.6 and 1.8 V. The rate in the channel (source) region indicates the generation of electrons (holes).

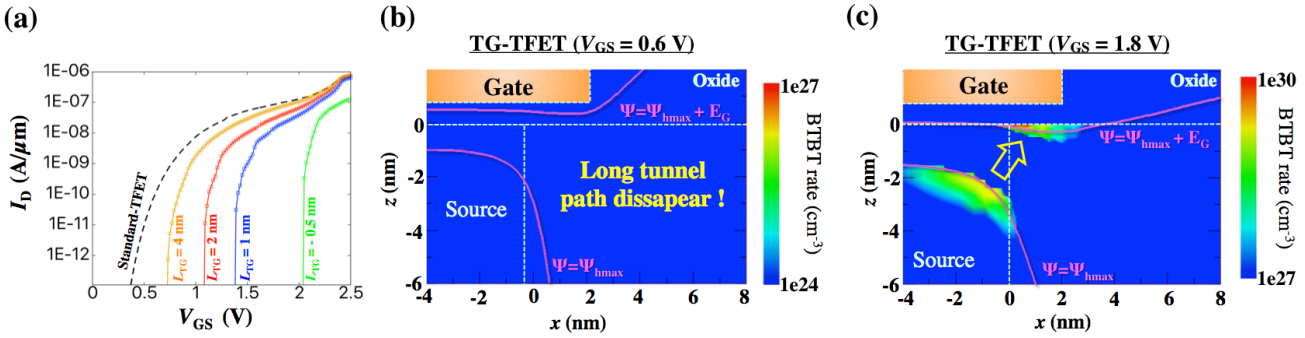


Fig. 3. (a) I_D as a function of V_{GS} for the TG-TFET. (b), (c) The distribution of the BTBT generation rate near the source in the TG-TFET with L_{TG} = 2 nm for V_{GS} = 0.6 and 1.8 V. The rate in the channel (source) region indicates the generation of electrons (holes).

small (V_{GS} = 0.6 V). As shown in Fig. 3(b), the contour line for $\Psi = \Psi_{hmax} + E_G$ moves away from the channel by the gate trimming, and the tunneling path to the channel region vanishes. Since the tunnel distance from the source edge to the channel is greater than L_{TG} when V_{GS} is small (Compare Fig. 2(b) with Fig. 3(b)), the destinations of the tunneling are out of the gate electrostatic control in the TG-TFET. Consequently, the BTBT current sharply increases with the sudden appearance of the short tunneling path under the high V_{GS} condition. In other words, the minor BTBT currents contributing to the off leak component of I_D is truncated by the TG structure.

Finally, we show a summary of the benefits of the TG structure in terms of *SS*. Figure 4 indicates average *SS* of TG-TFETs with N_{source} = 1×10^{20}, 2×10^{20} cm^{-3} as functions of L_{TG}. Here, we evaluated the average *SS* in the I_D range of 10^{-12} to 10^{-9} A/μm at V_D = 0.3 V. The dotted lines indicate the average *SS* for the Standard-TFETs as a reference. We can clearly see a significant improvement in the switching characteristics of TFETs owing to the TG structure. For the TG-TFET with N_{source} = 2×10^{20} cm^{-3}, the minimum average *SS* was 12.9 mV/decade at L_{TG} = -0.5 nm. Moreover, it can be seen that the *SS* improvement by the TG structure enhances with the increase in N_{source}. As the N_{source} increases, the width of the depletion layer on the source side decreases, and the hole populated region approaches to the gate edge. As a result, the length of the tunneling path truncated by the TG structure becomes short: the reduction of off leak component of the BTBT currents becomes remarkable.

4. Conclusion

In this paper, we proposed a novel TG structure, which realizes extreme steep switching in TFETs. We numerically

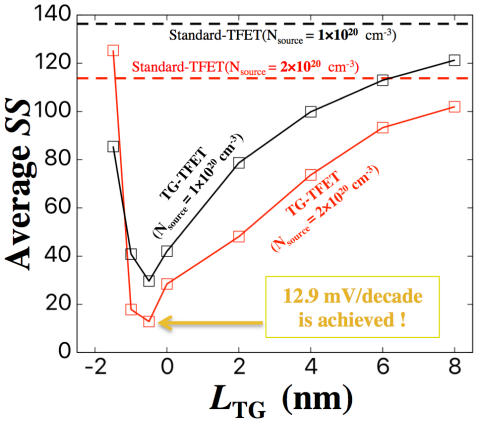


Fig. 4. Average *SS* of TG-TFETs as function of L_{TG}.

demonstrated that TG structure could achieve steep *SS* less than 15 mV/decade in an SOI TFET. A high source doping enhances the improvement of *SS* by the TG structure.

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References

[1] W. Y. Choi *et al.*, IEEE Electron Device Lett. **28** (2007) 743. [2] T. Mori *et al.*, Symp. VLSI Technol. Dig. Tech. Papers 2014, pp. 86 [3] T. Mori *et al.*, MRS Commun. **7** (2017) 541. [4] S. Iizuka *et al*, Mater. Sci. Semicond. Process. **70** (2017) 279. [5] S. Takagi *et al*, Symp. VLSI Technol. Dig. Tech. Papers 2015, pp. 22 [6] E. Memisevic *et al*, Nano Lett. **17** (2017) 4373. [7] H. Asai *et al.*, submitted to APEX[8] N. Kotani, Proc. Int. Conf. SISPAD 1998, p. 3. [9] T. Wada *et al*. Ext. Abstr. (53th Spring Meet. 2006), JSAP, 22p-ZA-2 [10] M. Nakamura, Oyo Buturi **77** (2008) 818.