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A Study of Interfacial Layer Quality and Thermal Stability of HfO_2/SiGe Gate Stack by Using NH_3 Plasma Treatment

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Abstract

We employed *in-situ* NH_3 plasma treatment to achieve high quality HfO_2/p-SiGe interface with the interface trap density (D_{it}) value down to 2.3×10^{11} $eV^{-1}cm^{-2}$. X-ray photoelectron spectra of the interfacial layer showed that the SiON layer was formed and no GeO_x existed in the interfacial layer. Moreover, post high-κ NH_3 plasma treatment enhanced the thermal stability and interfacial quality of SiGe MOS capacitors by preventing the diffusion of O atoms into SiGe substrate.

1. Introduction

SiGe alloy is shown to be a promising material for p-type MOSFETs due to its high carrier mobility and easy integration with the conventional Si technology. However, an undesired GeO_x formation and the emergence of Ge pile-up layer in high-κ/SiGe interface result in high density of interface traps (D_{it}) and low thermal stability. Nitridation is an effective method to passivate the SiGe surface before high-κ deposition. However, previous studies have focused only on improving the interfacial quality of SiGe with EOT > 2 nm [1-2].

In this study, we demonstrated NH_3 plasma treatment to improve the interfacial layer quality of SiGe MOS capacitor with EOT < 2 nm. Moreover, the interfacial quality and thermal stability of SiGe MOS capacitor can be improved by post high-κ NH_3 plasma treatment. Finally, we present XPS analysis to realize the material interaction as various processes.

2. Experiment

170-nm-thick $Si_{0.8}Ge_{0.2}$ substrates grown on (100) p-type Si wafer by LPCVD were used in the experiments. **Figs. 1(a) and (b)** illustrate the detailed process flow of the TiN/HfO_2/$Si_{0.8}Ge_{0.2}$/p-Si MOS capacitors and schematic structure of the SiGe MOS capacitor. First, the SiGe substrates were cleaned by using diluted HF and DI water for removing native oxides. Then, the *in-situ* passivation by NH_3 plasma treatment was conducted in ALD chamber prior to the high-κ layer deposition. Subsequently, the 60-cycle HfO_2 was deposited directly by thermal ALD at 250 °C. For the gate electrode, TiN was sputtered and patterned by using lift-off process. The backside contact was formed by Ti/Al deposition. After fabrication, post metallization annealing (PMA) was carried out at 300/400/500 °C for 1 min in N_2 ambient. For the case of EOT scaling, the deposition cycles of HfO_2 were reduced down to 30 cycles, and the post high-κ NH_3 plasma treatment was used.

3. Results and Discussion

Figures 2(a) and (b) show the multi-frequency C-V characteristics of the SiGe MOS capacitors with and without NH_3 plasma treatment with 60-cycle HfO_2 deposition. After NH_3 plasma treatment was used, D_{it} value extracted by conductance method was reduced from 1.2×10^{12} to 2.3×10^{11} $eV^{-1}cm^{-2}$. Moreover, the frequency dispersion in accumulation was improved from 7.9 to 5.0 % with NH_3 plasma treatment.

Then, we examined the XPS spectra of Si 2p and Ge 3d core levels to analyze the bonding state of the SiGe surface with and without NH_3 plasma treatment shown in **Fig. 3**. With NH_3 plasma treatment, the binding energy of Si-O bond for the Si 2p peaks shifted from 102.7 to 102.5 eV, which is consistent with the formation of SiON. In addition, the differences in the intensity of Si–O were attributed to IL thickness, which was proved by C-V characteristics shown in **Fig. 2**. Surprisingly, the Ge 3d peaks showed no GeO_x component after NH_3 plasma treatment. Conversely, the undesired GeO_x was formed in the case without NH_3 plasma treatment, which would result in the degradation of HfO_2/SiGe interface quality.

Figure 4 shows the multi-frequency C-V characteristics of the TiN/HfO_2 (30 cycles)/IL/SiGe for EOT scaling (from 1.6 to 1.3 nm). We also demonstrated the same process on Si substrates for comparison. When the temperature increased from 300 to 500 °C, the hump in the depletion region became severe due to the extra trap states generated, and the degradation of D_{it} value was shown in **Fig. 5**. Similarly, the Si MOS capacitors also followed this trend. To determine the changes in interface quality, XPS was performed on sample with 1 nm thick HfO_2 with different thermal annealing condition. **Fig. 6** shows the corresponding XPS spectra of the samples. The peak of Hf 4f core level of SiON/HfO_2 sample was shifted to lower binding energy, indicating that the O atoms tended to escape from HfO_2 layer after 500 °C thermal annealing. In addition, the Si 2p core level showed more Si-O bonds were formed. Therefore, we speculated that the escaped O atoms would diffuse through the SiON layer to react with SiGe substrate and degrade the interfacial quality of SiGe MOS capacitors. The schematic illustration of speculated behavior for O atoms was shown in **Fig. 7**. In order to improve the SiGe MOS capacitors, we applied post high-κ NH_3 plasma treatment to the HfO_2 layer. With this treatment, the D_{it} value decreased at three PMA temperature, and the less degradation as increasing the temperature from 300 to 400 °C was found as shown in **Fig. 5**. This indicates that post high-κ NH_3 plasma treatment on HfO_2 is a promising way to improve the interfacial layer quality and thermal stability of SiGe MOS capacitors.

4. Conclusions

In this study, we demonstrated NH_3 plasma treatment to improve the interfacial layer quality of SiGe MOS capacitor. We found that post high-κ NH_3 treatment can prevent O diffuse to SiGe substrate, result in improved D_{it} and thermal stability. NH_3 plasma treatment is a promising process to enhance the SiGe MOS capacitor quality and enable the fabrication of SiGe MOSFETs with thinner EOT.

Acknowledgement

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Reference

[1] K. Sardashti et al., Appl. Phys. Lett. 108, 011604 (2016).

[2] J.-H. Han et al., J. Appl. Phys. 120, 125707 (2016).

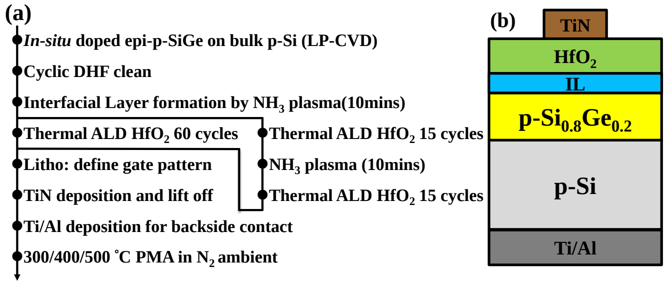

Fig. 1 (a) Process flow and (b) schematic structure of the SiGe MOS capacitor.

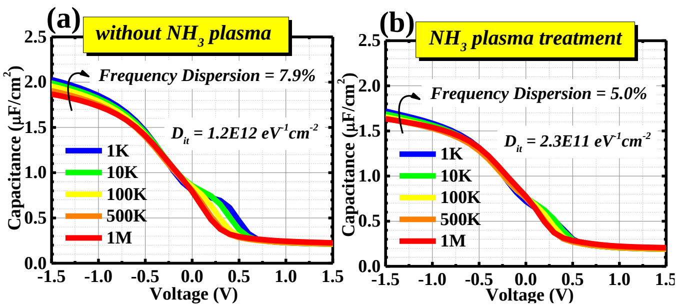

Fig. 2 C-V characteristics of the TiN/HfO_2 (60 cycles)/IL/SiGe MOS capacitors (a) without and (b) with NH_3 plasma treatment with PMA at 400 °C. D_{it} value was extracted by conductance method and frequency dispersion was calculated by $(C_{1K}-C_{1M})/C_{1K}$ in accumulation.

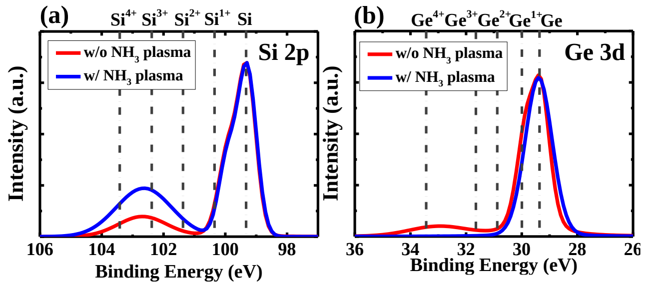

Fig. 3 Fitted XPS spectra of (a) Si 2p and (b) Ge 3d of the SiGe substrate with and without NH_3 plasma.

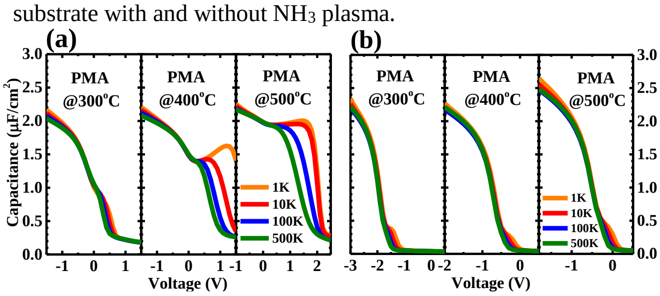

Fig. 4 C-V characteristics of the (a) SiGe and (b) Si MOS capacitors using 30-cycle HfO_2 for EOT scaling in different PMA temperature.

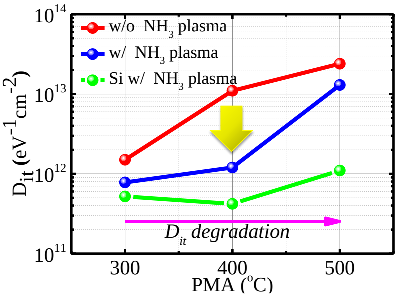

Fig. 5 Extracted D_{it} value of the SiGe MOS capacitors in different PMA temperature w/ and w/o post high-κ NH_3 plasma treatment.

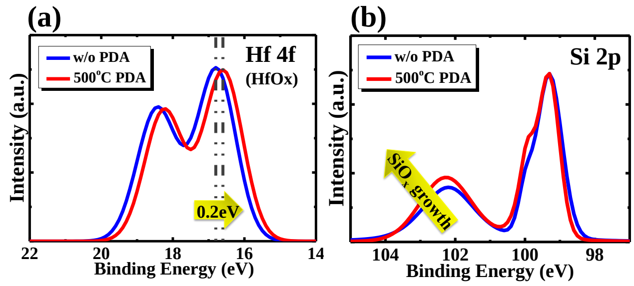

Fig. 6 Fitted XPS spectra of (a) Hf 4f and (b) Si 2p of the HfO_2 (1 nm)/SiGe samples w/ and w/o 500 °C thermal annealing.

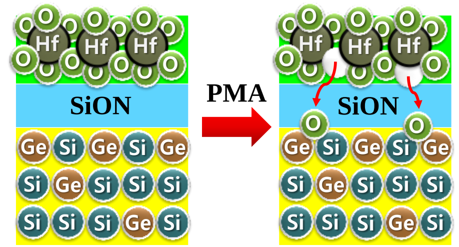

Fig. 7 Illustrative cartoon of the O diffusion behavior after PMA.