

Nanosheet Number and Width Optimization of Multi Stacked NanoSheet FET for 7-nm Node SoC Application

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Abstract

DC/AC performances of 7-nm node nanosheet FETs (NSFETs) having different the number of NS (N_{NS}) and NS widths (W_{NS}) were analyzed using calibrated TCAD. More N_{NS} increases on-currents and gate capacitances, but longer current paths for bottom-side NS reduce additional DC performance boosts. Smaller W_{NS} achieves better gate-to-channel controllability, but decreases current drivability by decreasing effective widths as a trade-off. RC delay of the NSFETs with different N_{NS} and W_{NS} was compared to 10-nm node FinFETs and optimized.

1. Introduction

FinFETs have been successfully scaled down to 10-nm node through 7-nm-thin fin for better short-channel effects (SCEs) and dummy gate removal for high density [1]. Meanwhile, nanosheet FETs (NSFETs) have been introduced as one of possible candidates to replace FinFETs in the sub-10-nm node [2]. Above all, three-stacked NSFETs having single wide NS width (W_{NS}) were suggested to increase effective width (W_{eff}) for high current drivability under the same device area [3]. However, there is no quantitative analysis of NS structure combined with source/drain (S/D) junctions in the sub-10-nm node for accurate power-performance optimization.

In this work, 7-nm node NSFETs with different the number of NS (N_{NS}) and W_{NS} have been analyzed using calibrated TCAD. Optimal structure of NSFETs for minimal RC delay was proposed including middle-of-line area.

2. Simulation Method

All the devices were simulated using Sentaurus TCAD. Doping, stress, interface, and ballisticity were considered for the calculation of carrier mobility. Fig. 1 shows fine calibration to 10-nm node FinFETs [1]. Larger S/D doping concentration and junction gradient (L_j) for PFETs are obtained to satisfy the subthreshold swing (SS) and drain-induced barrier lowering (DIBL) indicated at the bottom right of Fig. 1.

Fig. 2 shows the process flow of 7-nm node NSFETs referred from [2]. Si/Si_{0.7}Ge_{0.3} multi-layer epitaxy, Si_{0.7}Ge_{0.3} selective etching for inner-spacer formation, Poly-Si gate and Si_{0.7}Ge_{0.3} removals for HK/MG stack, and metal contacts for middle-of-line were executed successively. Geometrical parameters of 7-nm node NSFETs were indicated in Table I.

3. Results and Discussion

2-D cross sections of the three-stacked NSFETs were shown in Fig. 3. Double NSFETs ($W_{NS} = 16$ nm) were compared to single ones ($W_{NS} = 44$ nm) at the fixed device area

(FP×GP). On-currents (I_{on}) and gate capacitances (C_{gg}) of the NSFETs with different N_{NS} and W_{NS} were investigated for standard performance applications (off-current (I_{off}) = 0.1 nA) in Fig. 3. I_{on} and C_{gg} of 10-nm node FinFETs were also included for comparison. NFETs have larger I_{on} than do PFETs due to better SCEs by smaller L_j . Smaller L_j for NFETs also reduce parasitic capacitances (C_{para}) [4], having smaller increasing rate of C_{gg} with respect to N_{NS} than do PFETs. Wider W_{NS} is preferable to increase I_{on} by larger W_{eff} , but increases C_{gg} by intrinsic capacitances (C_{int}) and C_{para} . More N_{NS} increases W_{eff} , which increases C_{para} , C_{int} , and I_{on} , but the increasing rate of I_{on} with respect to N_{NS} becomes smaller.

This can be explained clearly in Fig. 4. Large amount of drain currents (I_{ds}) flow through the NS near the S/D contacts because the carrier path from source to drain contacts is short. The NSFETs have longer carrier paths for bottom-side NS, suffering from larger parasitic resistances (R_{sd}) of the S/D epi. This decreases contribution to the total I_{ds} of the NSFETs as the S/D epi height increases by more N_{NS} .

Fig. 5 shows the R_{sd} of the S/D epi and its extension as a function of N_{NS} . Total R_{sd} were extracted using Y-function [5], and contact resistances (R_{con}) of 50 Ω·μm for each S/D were subtracted from total R_{sd} . NFETs have larger R_{sd} than do PFETs due to smaller S/D epi and its extension doping concentrations. Larger W_{eff} by more N_{NS} or by larger W_{NS} decreases the R_{sd} , but its decreasing rate with respect to N_{NS} becomes smaller because of the larger S/D epi.

Fig. 6 summarizes the RC delay of 7-nm node NSFETs and 10-nm node FinFETs for three different applications. Minimum RC delay values are obtained at the N_{NS} of 2 and 3 for P- and NFETs, respectively. 7-nm node NSFETs have potential to decrease RC delay than 10-nm node FinFETs, but worse SCEs by short L_{sp} of 5 nm under the same L_j decrease performance boosts for low-power applications. PFETs have larger decreasing rate of C_{gg} than increasing rate of I_{on} with respect to N_{NS} , so the N_{NS} of 2 attains minimum RC delay. On the other hand, NFETs have smaller C_{para} from smaller L_j , which the I_{on} increase for the N_{NS} of 3 is larger than the C_{gg} increase and minimizes the RC delay for all three applications.

4. Conclusions

DC/AC performances of 7-nm node NSFETs with different N_{NS} and W_{NS} were investigated. Analyzing R_{sd} and C_{para} with respect to N_{NS} and W_{NS} , 7-nm node NSFETs have minimum RC delay smaller than 10-nm node FinFETs at the N_{NS} of 2 and 3 for p- and n-type devices, respectively.

Acknowledgements

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References

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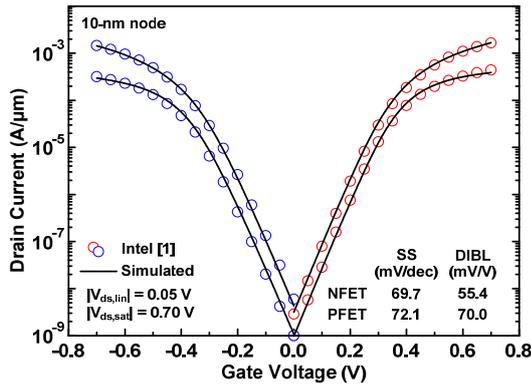


Fig. 1 Calibration of 10-nm node p/n bulk FinFETs.

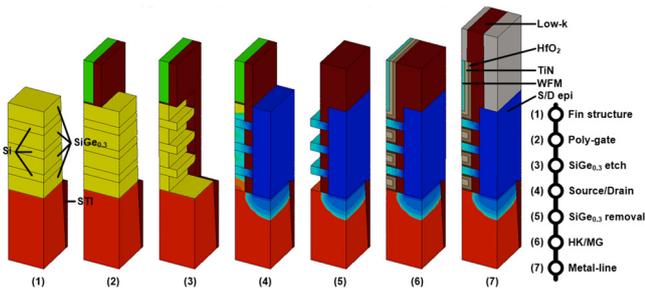


Fig. 2 Step-by-step simulated process flow of NSFETs.

Table I Geometrical parameters of 7-nm node NSFETs

Parameters	Symbols	Values
Fin pitch	FP	56 nm
Gate pitch	GP	44 nm
Gate length	L_g	12 nm
Spacer length	L_{sp}	5 nm
NS thickness	T_{NS}	5 nm
NS spacing	T_{SP}	10 nm
NS width	W_{NS}	16, 44 nm
The number of NS	N_{NS}	2, 3, 4, 5

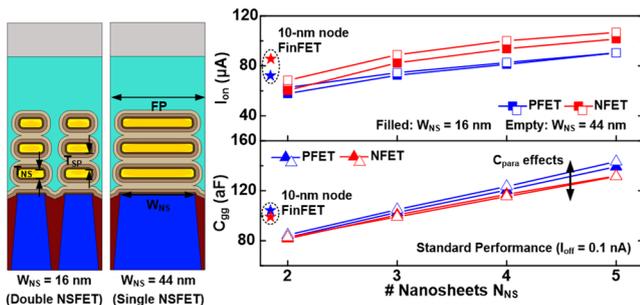


Fig. 3 Structure (left), and I_{on} and C_{gg} (right) of 7-nm node NSFETs.

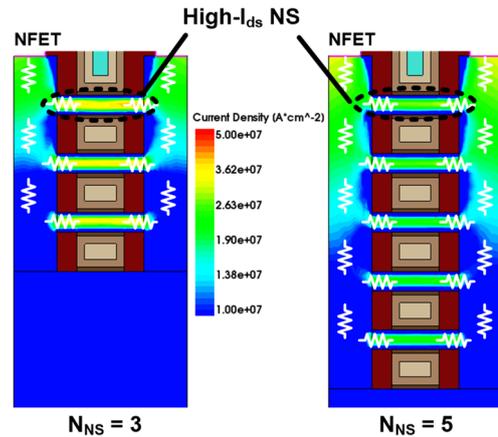


Fig. 4 I_{ds} density of NSFETs at on-state ($V_{gs} = V_{ds} = 0.7$ V)

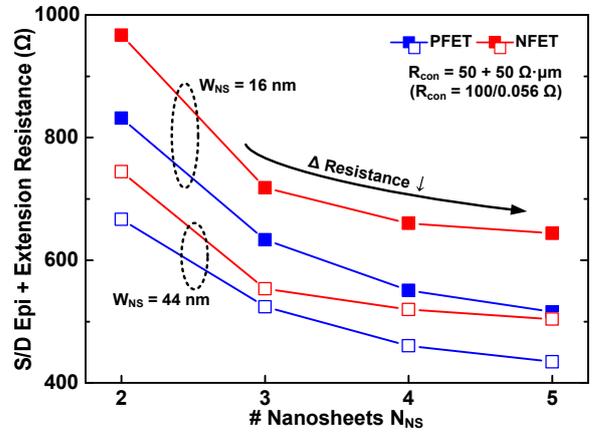


Fig. 5 S/D resistance of NSFETs with different N_{NS} and W_{NS} . Reduction of current boosting efficiency according to N_{NS} increase.

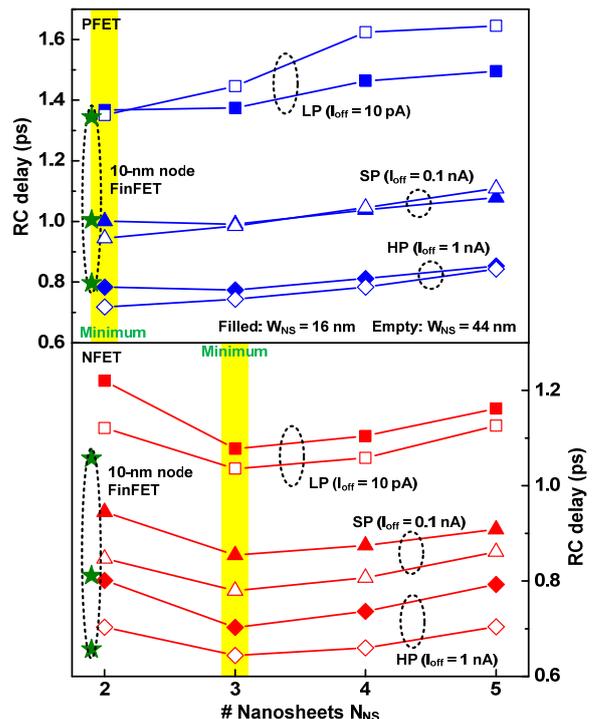


Fig. 6 RC delay of NSFETs with different N_{NS} and W_{NS} .