Extended Abstracts of the 2018 International Conference on Solid State Devices and Materials, Tokyo, 2018, pp879-880

Investigation of Gate-All-Around and Double-Gate InGaAs Negative-Capacitance FETs considering Quantum Capacitance

Shih-Han Lin, Shih-En Huang, and Pin Su
Department of Electronics Engineering & Institute of Electronics, National Chiao Tung University, Taiwan
E-mail: hannah.ee04g@nctu.edu.tw, toast.ee02g@nctu.edu.tw, pinsu@faculty.nctu.edu.tw

ABSTRACT

This work investigates the subthreshold characteristics and ON-state inversion charges (Q_{INV}) for gate-all-around (GAA) and double-gate (DG) InGaAs channel negative-capacitance FETs (NCFETs) considering quantum-confinement (QC) effects by using numerical simulation. Our study indicates that, albeit the quantum capacitance is beneficial to the subthreshold characteristics of NCFETs, its impacts on the ON-state internal gain and Q_{INV} boosting depend on the device structure. Compared with the Si counterpart, the InGaAs DG-NCFET with its step-like intrinsic inversion capacitance can get larger Q_{INV} boost induced by negative capacitance.

I. INTRODUCTION

Negative-Capacitance FET has been considered as a promising post-CMOS device candidate to achieve steep slope while maintaining a high enough current drive [2], [3]. With high electron mobility for n-FETs, InGaAs is a very attractive channel material. However, InGaAs possesses lower density-of-states (DOS), resulting in the loss of Q_{INV} and drive current for devices with small dimensions [4], [5]. For the NCFET, the internal gate voltage can be amplified (with gain Av). How might the action of negative capacitance affect the subthreshold characteristics and ON-state Q_{INV} for InGaAs NCFETs has rarely been known and merits investigation.

In this work, using TCAD numerical simulation [1], we investigate and compare GAA and DG NCFETs with In-GaAs/Si channel considering quantum-confinement effects.

II. METHODOLOGY

Fig. 1 shows the cross-sectional views of the GAA-NCFET and DG-NCFET structures with Si/InGaAs channel with the gate-oxide of the baseline GAA-MOSFET and DG-MOSFET replaced by a ferroelectric/metal/oxide stack. The device dimensions are based on the ITRS 2024 technology node [6]. For $In_{0.53}Ga_{0.47}As$, an isotropic effective mass is assumed ($m^*_{ch} = 0.041m_0$). For Si, surface orientation (100) is considered.

In this work, using TCAD numerical simulation that self-consistently solves the 2D Poisson and 1D Schrödinger equations, we extracted the I_d-V_G and Q_G-V_G data from the baseline GAA-MOSFET and DG-MOSFET, and coupled them with the 1D static LK equation [2]:

$$V_{FE} = T_{FE}(2\alpha Q_G + 4\beta {Q_G}^3 + 6\gamma {Q_G}^5) \quad (1)$$

In (1), T_{FE} is the ferroelectric thickness, α = -4.23E9 m/F, β = 4.07E12 $m^5/F/C^2$ and γ = 0 $m^9/F/C^4$ are the ferroelectric parameters (HfZrO) [7], and V_{FE} is the voltage drop across the ferroelectric.

III. RESULTS AND DISCUSSION

Fig. 2 shows that, the intrinsic inversion capacitance (C_{INV}) of the GAA InGaAs MOSFET exhibits a non-monotonic behavior [4] due to its 1D DOS nature. With decreasing channel thickness (T_{CH}), the 2D QC effect becomes stronger and the number of C_{INV} peaks becomes fewer. Moreover, in subthreshold region, the GAA InGaAs NCFET with T_{CH} = 4 nm can achieve the highest Av among the three channel thicknesses.

Fig. 3 shows the capacitance matching for the GAA-MOSFET with InGaAs/Si channel. Due to its lower DOS, the C_{INV} of the InGaAs channel is lower than that of the Si channel, resulting in higher Av for InGaAs channel. Fig. 4 shows the subthreshold I-V for GAA-MOSFETs and GAA-NCFETs with InGaAs/Si channel. Due to its higher Av, the GAA InGaAs NCFET can achieve lower average SS ($SS_{NC} = SS_{MOS}/Av$) than the Si channel.

With the action of negative capacitance, the ON-state Q_{INV} can also get boosted. Fig. 5 compares the Q_{INV} vs. gate-voltage overdrive (V_{GT}) for the GAA-MOSFETs and GAA-NCFETs with InGaAs/Si channel. It can be seen that, the Q_{INV} enhancement due to negative capacitance for the GAA Si channel is larger than the InGaAs channel. This is because the C_{INV} of the InGaAs channel exhibits the non-monotonic one-peak behavior, resulting in the rapid decrease in Av at ON-state (Fig. 3).

Fig. 6 shows the capacitance matching for the DG-MOSFET with InGaAs/Si channel. Due to the 1D QC effect, the C_{INV} of the InGaAs channel is step-like and lower than that of the Si channel. Fig. 7 shows that the DG InGaAs NCFET can achieve lower average SS than the Si counterpart due to its higher Av. Fig. 8 shows that the step-like C_{INV} of the InGaAs channel significantly extends the high Av region at ON-state (Fig. 6). Hence, for the DG-NCFET, the InGaAs channel can get larger Q_{INV} boost than the Si channel.

Fig. 9 (a) and (b) futher compare the Q_{INV} ratio of Si to InGaAs ($Q_{INV,Si}/Q_{INV,InGaAs}$) for the GAA and DG structures, respectively. It can be seen from Fig. 9 (b) that the $Q_{INV,Si}/Q_{INV,InGaAs}$ for the DG-NCFET is significantly lower than that of the DG-MOSFET due to the Q_{INV} boosting mechanism induced by negative capacitance.

ACKNOWLEDGEMENT

This work is supported in part by the Ministry of Science and Technology, Taiwan, under MOST 106-2221-E-009-148-MY2, MOST-107-2633-E-009-003, and MOST-107-3017-F-009-002.

REFERENCES

[1] *ATLAS,* SILVACO. [2] S. Salahuddin and S. Datta, *Nano Lett.,* vol. 8, no. 2, pp. 405-410, 2008. [3] K.-S. Li et al., *IEDM Tech. Dig.*, p. 616, 2015. [4] H.-H. Shen et al., *IEEE TED*, vol. 63, no. 1, 2016. [5] S.-L. Shen et al., *Extended Abstracts SSDM*, pp. 44-45, Sep. 2015. [6] ITRS (http://www.itrs.net/). [7] M. Kobayashi and T. Hiramoto, *VLSI Symp. Tech. Dig.*, pp. T212-T213, Jun. 2015.

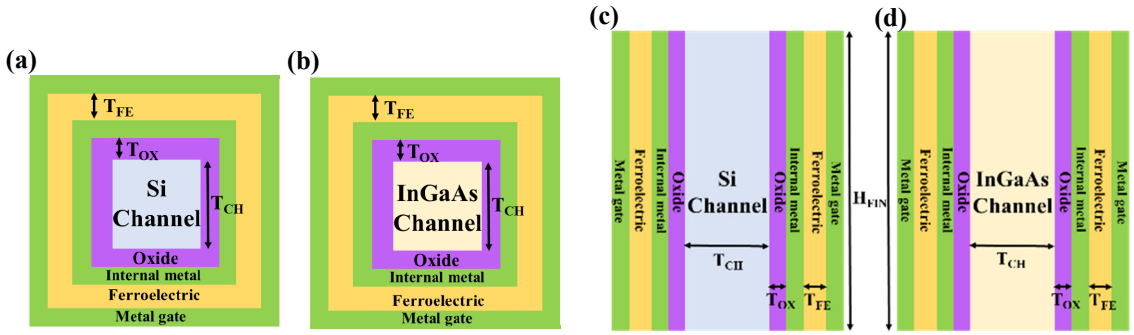

Figure 1. Schematic cross sectional views of (a) Si GAA, (b) InGaAs GAA, (c) Si DG, and (d) InGaAs DG NCFETs in this study.

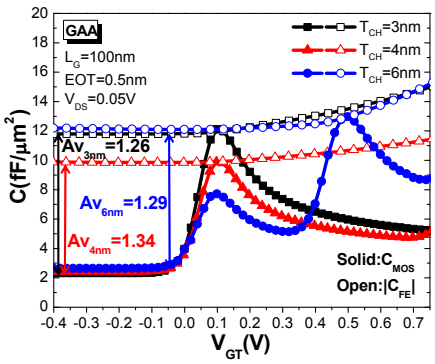

Figure 2. Capacitance matching of the GAA InGaAs MOSFET with various T_{CH}. Av = $|C_{FE}|/(|C_{FE}|-C_{MOS})$.

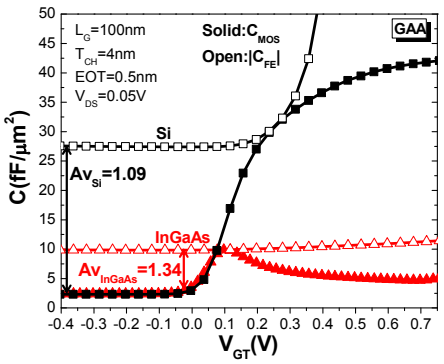

Figure 3. Capacitance matching of the GAA-MOSFET with Si and InGaAs channel, respectively.

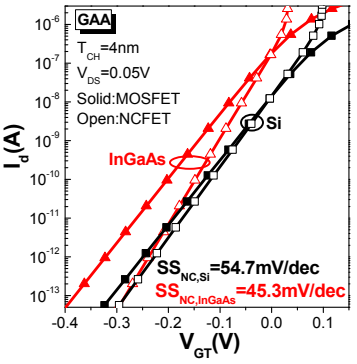

Figure 4. Subthreshold I-V for InGaAs/Si GAA MOSFETs and NCFETs. T_{FE} = 4.3 nm and 11.2 nm for Si and InGaAs channels, respectively.

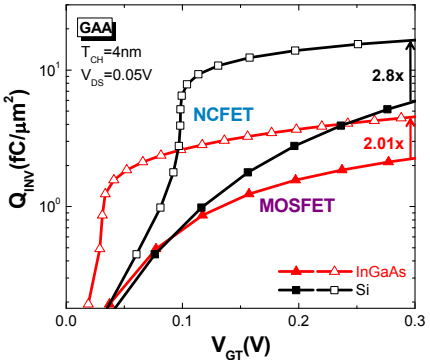

Figure 5. Comparison of Q_{INV} characteristics for GAA MOSFETs and NCFETs with Si and InGaAs channel.

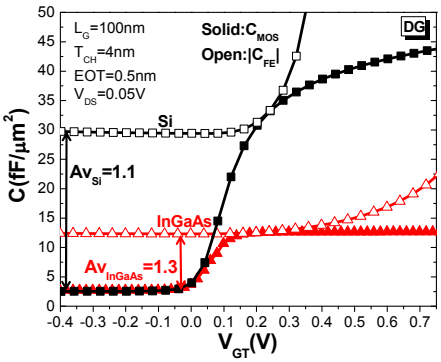

Figure 6. Capacitance matching of the DG-MOSFET with Si and InGaAs channel, respectively.

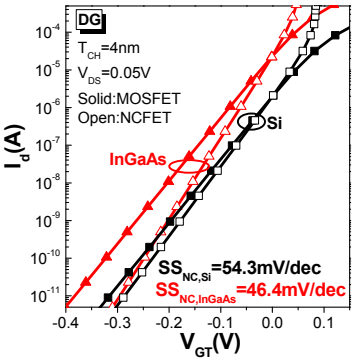

Figure 7. Subthreshold I-V for InGaAs/Si DG MOSFETs and NCFETs. T_{FE} = 4 nm and 9.6 nm for Si and InGaAs channels, respectively.

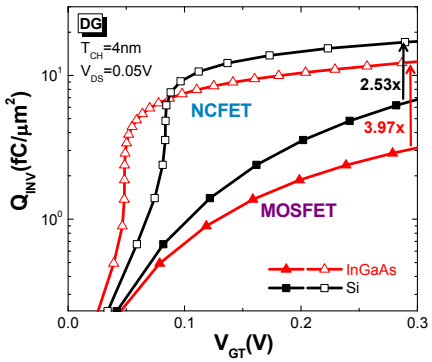

Figure 8. Comparison of Q_{INV} characteristics for DG MOSFETs and NCFETs with Si and InGaAs channel.

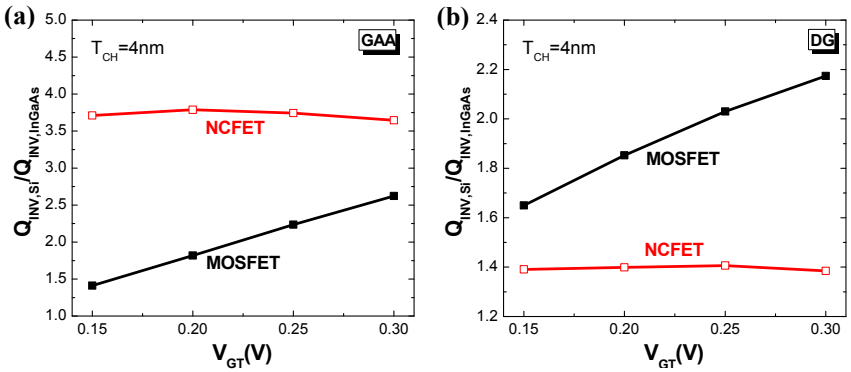

Figure 9. Q_{INV} ratio of Si to InGaAs channel with varying gate-voltage overdrive for (a) GAA structures, and (b) DG structures.