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# Improvement of $I_{ON}$ and *S.S.* values of p-$GaAs_{0.51}Sb_{0.49}$/$In_{0.53}Ga_{0.47}As$ hetero-junction vertical TFETs by using abrupt source impurity profile

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## Abstract

**Effects of source impurity concentrations and profiles on electrical characteristics of Be- or C-doped p-$GaAs_{0.51}Sb_{0.49}$/$In_{0.53}Ga_{0.47}As$ vertical TFETs are experimentally studied. The GaAsSb/InGaAs TFETs are mainly characterized at 50 K in order to suppress the trap-related generation/recombination leakage current. The $I_{ON}$ and *S.S.* are improved by using C instead of Be as the source impurity, attributed to the much steeper C profile near the source/channel interface than the Be one. The $I_{ON}$ of $1.7 \times 10^{-6}$ A/$\mu$m at $V_D$ = 500 mV and $V_G$ = 1.5 V is obtained. The minimum *S.S.* of ~ 20 mV/dec. is achieved at $V_D$ = 50 mV. These results suggest that GaAsSb/InGaAs TFETs are promising for an ultralow power switching device.**

## 1. Introduction

Tunnel field effect transistors (TFETs) have widely been studied as promising candidates for steep slope devices [1]. However, it is well known that it is difficult to obtain high $I_{ON}$ and low *S.S.* at the same time. While various types of TFETs have been proposed to overcome this problem, a type-II hetero-junction TFET is one of the most promising structures [2, 3]. The type-II band alignment allows us to design the optimal combination of the source and channel materials for reducing the tunnel width ($\lambda$) with maintaining large bandgap ($E_g$) and the low leakage current. Among a variety of type-II hetero-interfaces, Ga(As)Sb/ In(Ga)As hetero-junctions can provide relatively low effective barrier height ($E_{b\_eff}$). Actually, p-GaAsSb/InAs vertical nano-wire n-TFETs demonstrated the minimum *S.S.* of 48 mV and $I_{ON}$ of 10.6 $\mu$A/$\mu$m at $V_D$ of 0.3 V [4], strongly suggesting the high potential of Sb-based TFETs.

So far, we have reported p$^+$-$GaAs_{0.51}Sb_{0.49}$/ $In_{0.53}Ga_{0.47}As$ hetero-junction vertical tunnel field effect transistors on InP substrates with *S.S.* of ~ 80 mV/dec [5]. In order to clarify the critical factors to determine the TFET characteristics such as *S.S.* and $I_{ON}$, we have analyzed the device characteristics by the 2-dimensional device simulation using the composition and impurity profiles, experimentally obtained. It has been, as a result, found that the concentration and abruptness of the source impurities significantly affect *S.S.* and $I_{ON}$.

In this study, we experimentally investigate the effects of the source impurity concentration and profile on the electrical characteristics of vertical Be- and C-doped $GaAs_{0.51}Sb_{0.49}$/$In_{0.53}Ga_{0.47}As$ TFETs on InP substrates for obtaining low *S.S.*

## 2. Experimental procedure

The schematic structure of a GaAsSb/InGaAs vertical TFET and the process flow are shown in Fig. 1. The Be-doped and C-doped p$^+$-$GaAs_{0.51}Sb_{0.49}$ on un-doped $In_{0.53}Ga_{0.47}As$ ($N_D$ ~ $4\times10^{16}$ cm$^{-3}$) were successively grown on InP substrates ($N_D$ = ~ $5 \times 10^{18}$ cm$^{-3}$) by metal-organic molecular beam epitaxy (MOMBE) and metal-organic chemical vapor deposition (MOCVD), respectively. Here, the source Be concentrations evaluated by Hall measurements are $1 \times 10^{19}$ and $4 \times 10^{19}$ cm$^{-3}$, while the C concentrations are $4 \times 10^{19}$, $7 \times 10^{19}$ and $1 \times 10^{20}$ cm$^{-3}$. The isolation and source region patterning were conducted by wet etching of $H_3PO_4$ : $H_2O_2$ : $H_2O$ (1 : 1 : 7). A 10-nm-thick ALD $Al_2O_3$ was deposited at relatively low temperature of 150 °C as a gate insulator after the pre-cleaning using an $(NH_4)_2S_x$ solution for 1 min. Here, EOT is ~ 5.8 nm. Then, Ta gate, Ni/Pt source and Au drain contacts were formed. The depth profile of impurities and the composition atoms were evaluated by SIMS using Cs$^+$ ions.

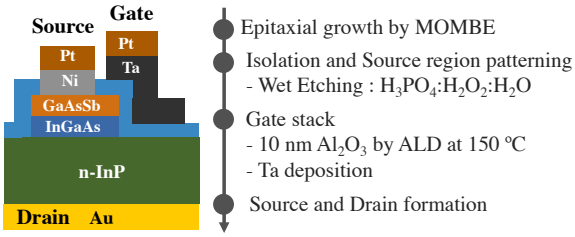


Fig.1 Schematic structure of a GaAsSb/InGaAs vertical TFET with process flow sequences.

## 3. Result and discussion

Fig. 2 shows the $I_D$–$V_G$ characteristics of fabricated TFETs using Be-doped GaAsSb/InGaAs, grown by MOMBE, with source $N_A = 1 \times 10^{19}$ and $4 \times 10^{19}$ cm$^{-3}$, measured at 293 and 50 K. The *S.S.*–$I_D$ characteristics at 50 K are also shown. The strong temperature dependence of $I_D$ in the subthreshold region and *S.S.* is observed. The *S.S.* values at 50 K are improved thanks to suppressing the trap-related generation/recombination leakage current. The minimum *S.S.* value of ~ 80 mV/dec. is obtained. Regarding the $I_D$–$V_G$ and *S.S.* characteristics at 50 K of the GaAsSb/InGaAs TFET, no difference is observed between the source impurity concentration of $1 \times 10^{19}$ and $4 \times 10^{19}$ cm$^{-3}$. Fig. 3 shows the $I_D$–$V_G$ characteristics and the *S.S.*–$I_D$ characteristics of fabricated TFETs using C-doped GaAsSb/InGaAs, grown by MOCVD, with source $N_A = 4 \times 10^{19}$, $7 \times 10^{19}$ and $1 \times 10^{20}$ cm$^{-3}$ at 50 K. The minimum *S.S.* value of ~ 20 mV/dec. is achieved at $V_D$ = 50 mV and the ON/OFF ratio of ~ $10^7$ in the $V_G$ swing of 1.25 V is obtained. Almost no difference in the electrical characteristics is observed among the different

source concentrations. Fig. 4 compares the $I_D$–$V_G$ characteristics and the *S.S.* characteristics between the Be- and C-doped GaAsSb/InGaAs TFETs with the same source Hall concentration of $4 \times 10^{19}$ cm$^{-3}$. It is clearly found that the $I_{ON}$ and *S.S.* improve by using C instead of Be as the source impurity. Fig. 5 summarizes $I_{ON}$ at $V_G = 1.5$ V and *S.S.* at $I_D = 1 \times 10^{-11}$ A/$\mu$m of the Be- and C-doped GaAsSb/InGaAs TFETs. It is found that the C-doped source GaAsSb/InGaAs TFETs exhibit the better performance. In the current device structure, the source impurity concentration less affects the electrical characteristics of the GaAsSb/InGaAs TFETs. As a result, the source concentration of $4 \times 10^{19}$ cm$^{-3}$ is sufficient for obtaining the good electrical characteristics of the present TFETs.

In order to understand the physical origin of these results, we have characterized the source impurity profile by SIMS analysis with $Cs^+$ ions. Fig. 6 and 7 show the SIMS profiles of Be and C atoms, respectively, as the source impurity and As atoms in the GaAsSb/InGaAs hetero-junctions. The As intensity rapidly changes at the source/channel interface. In both the Be and C profiles, the maximum SIMS concentrations changes, dependent on the doping concentrations evaluated by Hall measurements, while the abruptness of the profiles has almost no difference. The abruptness of the Be and C profiles is estimated to be 11 and 8 nm/dec., respectively, suggesting that the abruptness in the source impurity profiles strongly affects the $I_D$–$V_G$ and *S.S.* characteristics shown in Fig. 2, 3, 4 and 5.

Fig. 8 shows the activation energy estimated from the temperature dependence of the $I_D$–$V_G$ curves of the Be- and C-doped GaAsSb/InGaAs TFETs as a function of $V_G$, which can be related to the crystallinity of the hetero-junctions. This result means that the quality of C-doped GaAsSb/InGaAs junction is lower than Be-doped one. We can conclude, as a result, that the critical factor to determine the TFET characteristics is the source abruptness rather than the quality of the crystallinity of the hetero-junctions.

## 4. Conclusions

We fabricated and characterized Be- and C-doped $GaAs_{0.51}Sb_{0.49}/In_{0.53}Ga_{0.47}As$ TFETs in order to experimentally examine the effects of the source impurity concentration and profile. Moreover, the quality of source/channel junctions were evaluated from the activation energy. As a result, it is found that the source abruptness is the most affective factor to determine the TFET characteristics rather than the impurity concentration and the quality of source/channel junction. Thanks to the abrupt impurity profile in the source/channel hetero-junction by using C instead of Be as the source impurity, the $I_{ON}$ of $1.7 \times 10^{-6}$ A/$\mu$m at $V_D = 500$ mV and the minimum *S.S.* value of ~ 20 mV/dec. at $I_D = 1 \times 10^{-11}$ A/$\mu$m at $V_D = 50$ mV are achieved.


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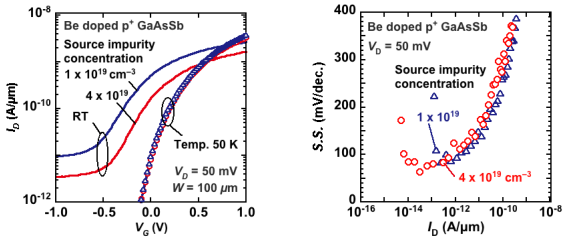


Fig. 2 (Left) $I_D$–$V_G$ curves of Be-doped p$^+$GaAsSb/InGaAs TFETs at RT and 50 K and (Right) *S.S.*–$I_D$ characteristics at 50 K. Here, source impurity concentration are $1 \times 10^{19}$ and $4 \times 10^{19}$ cm$^{-3}$.

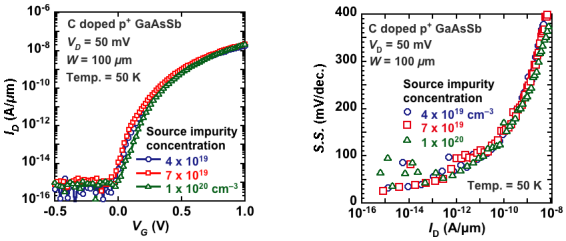


Fig. 3 (Left) $I_D$–$V_G$ curves of C-doped p$^+$GaAsSb/InGaAs TFETs and (Right) *S.S.*–$I_D$ characteristics at 50 K. Here, source impurity concentration are $4 \times 10^{19}$, $7 \times 10^{19}$ and $1 \times 10^{20}$ cm$^{-3}$, respectively.

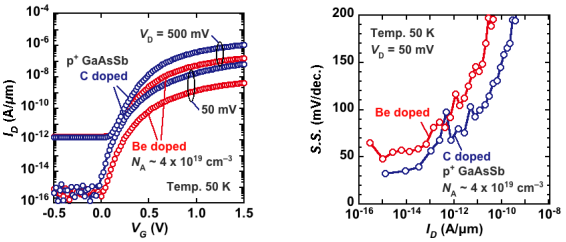


Fig. 4 $I_D$–$V_G$ curves of Be- and C-doped p$^+$GaAsSb/InGaAs TFETs at 50 K with $N_A = 4 \times 10^{19}$ cm$^{-3}$.

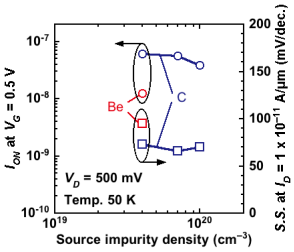


Fig. 5 Summary of $I_{ON}$ at $V_D = 0.5$ V and *S.S.* at $1 \times 10^{-11}$ A/$\mu$m of Be- and C-doped GaAsSb/InGaAs TFETs with Hall concentrations of $4 \times 10^{19}$, $7 \times 10^{19}$ and $1 \times 10^{20}$ cm$^{-3}$.

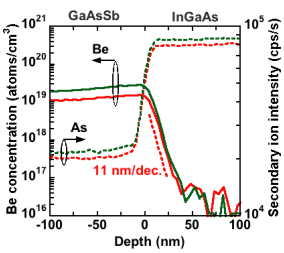


Fig. 6 SIMS profiles of Be atoms as the source impurity and As atoms in the GaAsSb/InGaAs hetero-interfaces.

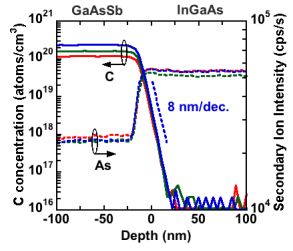


Fig. 7 SIMS profiles of C atoms as the source impurity and As atoms in the GaAsSb/InGaAs hetero-interfaces.

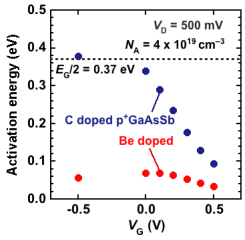


Fig. 8 Activation energy of Be- and C-doped GaAsSb/InGaAs TFETs at 50 K.