Extended Abstracts of the 2018 International Conference on Solid State Devices and Materials, Tokyo, 2018, pp1239-1240

Loading Effect in the Channel Etching Process of Crystalline In-Ga-Zn-Oxide FETs

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Abstract

In Si LSI fabrication, a phenomenon is known in which loading or microloading effect affects the etching rate or shape in the plasma etching process. Also in a memory including FETs employing c-axis aligned crystalline indium-gallium-zinc oxide (CAAC-IGZO), a crystalline oxide semiconductor, loading effect in which pattern density influences the etching performance in the channel etching process is observed. Accordingly, there is a concern that variations in the etching amount of CAAC-IGZO where a channel is formed cause variations in FET characteristics. Thus, the range affected by the loading effect is examined and a minimum required number of dummy FETs are provided around the memory. As a result, channel regions of CAAC-IGZO FETs can be uniformly etched while an increase in chip size is minimized.

1. Introduction

In recent years, FETs using c-axis-aligned crystalline indium-gallium-zinc oxide (CAAC-IGZO) have been researched for use in backplanes of LCDs and OLED displays [1,2]. In addition, application of the CAAC-IGZO FETs to memories, CPUs, and FPGAs has also been studied [5]. The CAAC-IGZO FET has a feature of low off-leakage current [3,4]; thus, low-power-consumption devices utilizing the feature would be feasible. Furthermore, a CAAC-IGZO FET with a channel length in the order of 60 nm exhibited FET characteristics [5-8], and further miniaturization and integration are desired.

In Si LSI, loading or microloading effect is known in which the pattern density or the aspect ratio affects etching performance in the plasma etching process of forming trenches for, for example, trench capacitors or word lines [9]. Also in CAAC-IGZO LSI (oxide semiconductor (os) LSI), the influence of loading effect on the FET fabrication process should be comprehended for further integration and mass production. We found that the loading effect influences the osLSI process as well as the Si LSI process.

2. Loading Effect

Even under the same plasma etching conditions, etching rate or etching shape varies depending on the etching area or the pattern density. This phenomenon is called loading effect. When the amount of an etchant (radicals, reactive ions) is constant but the etching area is increased, the consumption of the etchant is increased and the etching rate is decreased by a shortage of the etchant. Therefore, the loading effect is a non-negligible factor of variations in the VLSI process; for example, uniformity of the etching amount is decreased depending on the layout.

3. Trench Gate Formation Process

A device structure employed in this study is based on the trench-gate self-aligned structures shown in references [7,8] (Fig. 1).

In the process of forming a trench gate of the trench-gate self-aligned structure, a trench layer (interlayer insulating film) is etched and then source and drain (S/D) electrodes are formed by etching. For the S/D electrodes, TaN_x is employed. An inductively coupled plasma (ICP) etching apparatus is used for the S/D electrodes formation etching. As the etching gases, Cl_2 and Ar are used. The substrate temperature is set to 40°C. Thus, the TaN_x/CAAC-IGZO etching selectivity is approximately 25.

In the etching process of the TaN_x S/D electrodes over the channel, appropriate over-etching needs to be performed in order not to generate TaN_x etching residue while etching of the CAAC-IGZO film where the channel is formed is minimized. Even when the TaN_x/CAAC-IGZO etching selectivity is approximately 25, the etching amount of the channel region by the over-etching varies over the wafer in some cases because of the loading effect, which might cause variations in FET characteristics and a decrease in reliability.

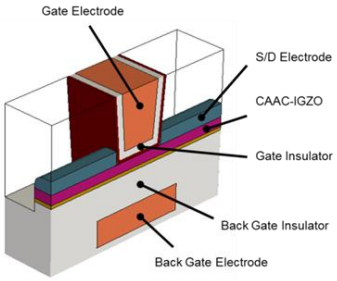

Fig. 1 Trench-gate self-aligned structure.

4. Experiment Method

In the field of Si LSI, it is known that providing dummy FETs to make layout density uniform is effective in suppressing the loading effect. In this study, whether the loading effect affects the channel etching process in the osLSI, and if it does, whether the influence thereof can be suppressed by providing dummy FETs around a single FET were examined.

To examine the loading effect, a test element group (TEG) of CAAC-IGZO FETs arranged in 132 rows × 132 columns was fabricated by providing dummy FETs around a

single CAAC-IGZO FET to simulate a memory. Fig. 2 shows schematic diagrams of the TEG used for the experiment.

Cross-sectional observation using a scanning transmission electron microscope (STEM) was performed on some of FETs from the outermost FET (in the first row and first column) to the center single FET of the fabricated TEG, and the etching amounts of the channel regions were measured.

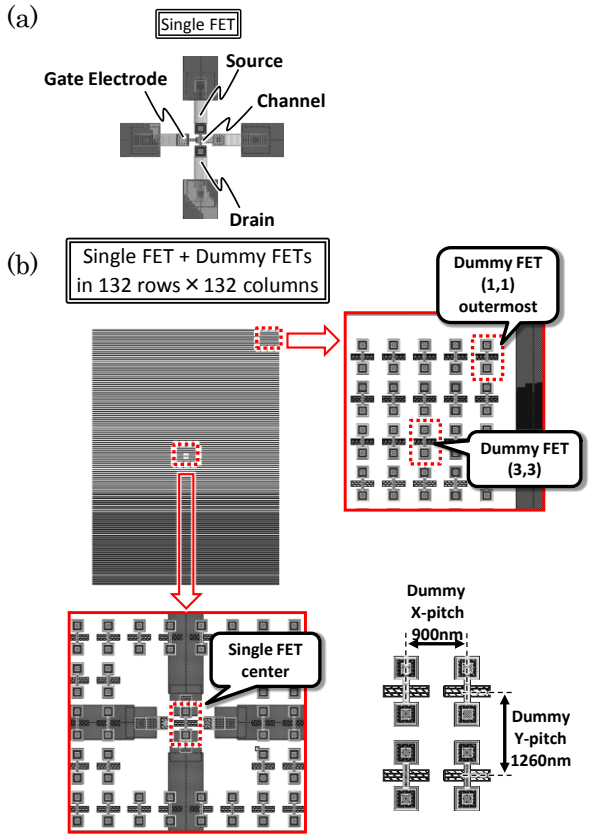

Fig. 2 Schematic diagrams of TEG used for loading effect examination. (a) Top view of single FET, (b) Top view of single FET and dummy FETs.

5. Cross-sectional Observation Results

Fig. 3 shows the results of the cross-sectional observation of the TEG. Fig. 4 shows the etching amounts of CAAC-IGZO channel regions (layout dependence). The results indicate that the etching amount of the channel region varies depending where the dummy FET is positioned. Specifically, the etching amount of the outermost dummy FET (in the first row and first column) is the largest, whereas the etching amounts of the FETs from the third row and third column to the center are substantially uniform. Furthermore, the etching amount of the channel region of the single CAAC-IGZO FET around which dummy FETs are not provided is substantially equal to that of the outermost dummy FET (in the first row and first column). Thus, the loading effect in the channel etching process was suggested in the fabricated TEG including CAAC-IGZO FETs arranged in 132 rows × 132 columns. Moreover, providing dummy FETs is effective in suppressing the loading effect in the osLSI process.

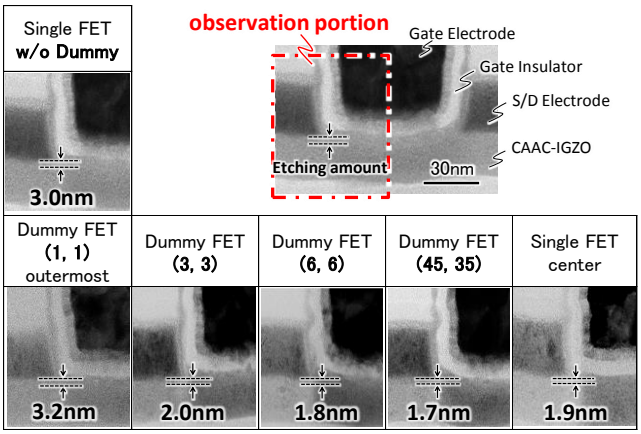

Fig. 3 Cross-sectional STEM image of FET used for loading effect examination.

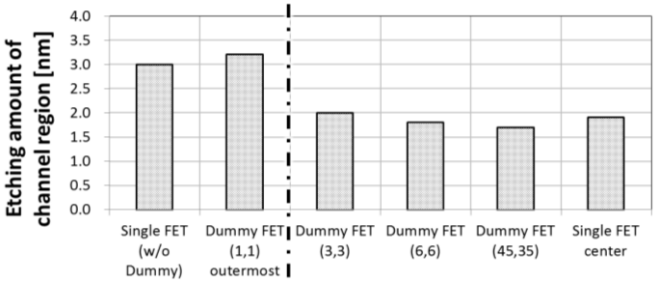

Fig. 4 Etching amounts of CAAC-IGZO channel regions (layout dependence).

6. Conclusions

As miniaturization and integration of CAAC-IGZO FETs progress, the FETs are expected to be used not only in displays but also in LSI circuits. The loading effect in the osLSI process was examined with the use of the TEG fabricated to simulate a memory including minute CAAC-IGZO FETs on the assumption of mass production. Also in the osLSI process, the loading effect, which causes variations in etching performance, was observed. The region where the loading effect influences was also determined.

The above results suggest that by providing dummy FETs as appropriate, variations in etching performance can be suppressed and uniform channel etching can be performed.

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