

Improved Electrical Stability of Zr-IGZO Thin-Film Transistors with $\text{Zr}_{0.85}\text{Si}_{0.15}\text{O}_2$ Gate Dielectric

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Abstract:

The use of RF co-sputtering to incorporate zirconium (Zr) in IGZO channel to reduce the oxygen vacancies, improved performance of zirconium doped indium gallium zinc oxide thin-film transistors (Zr-IGZO TFTs) with zirconium silicon oxide ($\text{Zr}_{0.85}\text{Si}_{0.15}\text{O}_2$) as gate dielectrics is demonstrated. The proposed Zr-IGZO TFTs show a much better reliability than that of conventional IGZO TFTs under positive and negative gate bias stresses (PGBS and NGBS). Experimental results reveal that Zr-IGZO channel deposited at a power ratio of IGZO:ZrO₂=80 W:50 W and post deposition annealed (PDA) in N₂ shows the best device performance such as the on/off current ratio of 1.59×10^8 , the subthreshold swing of 96 mV/dec, and the threshold voltage shift after 1000 sec positive/negative gate bias stress of 0.36 V/-0.23 V, respectively.

1. Introduction

For having wide band gap, high field effect mobility, room temperature deposition, and high uniformity over large areas, amorphous indium gallium zinc oxide (α -IGZO) has attracted considerable attention in the fabrication of thin-film transistors (TFTs) for active-matrix flat-panel display applications [1-3]. Nevertheless, owing to interstitial zinc atoms and oxygen vacancies from weak In-O bonds in α -IGZO channel, α -IGZO TFTs usually encounter reliability issue caused by charge trapping via internal or external defect states. Instability in electrical characteristics of TFTs might result in incorrect gray scales which further affected the screen performance quality [4].

However, previous studies indicated that H₂O molecules and oxygen would be adsorbed onto the oxide semiconductor layer back surface for the bottom gate α -IGZO TFT without a passivation layer [6]. So, the sputtered SiO₂ acted as the passivation layer to block the oxygen and H₂O molecules from ambience to ensure α -IGZO TFT stability.

Zirconium (Zr) has a larger oxygen vacancy formation energy (8.8 eV) than Zinc and possesses a high Zr-O bonding energy (776.1 kJ Mol) [5], suppression of charge carrier trapping to improve device stability through a suitable incorporation of zirconium ions (Zr^{4+}) as a carrier suppressing dopant in α -IGZO channel layer can be expected. In this study, a co-sputtering process with IGZO and ZrO₂ targets at room temperature (RT) is proposed to incorporate Zr with α -IGZO. The use of sputtered SiO₂ to passivate device structure to block possible oxygen and H₂O molecules adsorbed from ambient to further strengthen α -IGZO TFT stability is demonstrated. Effect of Zr content in α -IGZO channel on device performance and reliability is analyzed. The optimum RF power ratio and post deposition annealing (PDA) to realize a suitable Zr content in α -IGZO channel for TFT applications is proposed. Results of threshold voltage shift ΔV_{TH} obtained from positive and negative bias stress tests are presented and discussed.

2. Experimental

Figure 1 depicts the schematic cross section view of the fabricated Zr-IGZO TFT with a co-sputtering of ZrO₂ and SiO₂ in Ar ambient at RT. The fabrication process begins with the deposition of $\text{Zr}_{0.85}\text{Si}_{0.15}\text{O}_2$ gate dielectric layer with a thickness of 9 ± 1 -nm-EOT layer, followed by a post deposition annealing (PDA in O₂ at 600 °C) for 10 min on an n⁺-Si substrate [7]. Then a 25-nm-thick active channel layer Zr-IGZO was deposited by co-sputtering of IGZO and ZrO₂ target in Ar ambient at RT. To investigate the influence of Zr content on channel performance, various sputtering powers (0, 30, 50 and 80 W) were used for the ZrO₂ target with

that of the IGZO target kept at 80 W during sputtering deposition. For comparisons, two groups of channel layers with and without a post-deposition annealing (PDA) at 300 °C in nitrogen (N₂) ambient for 10 min were prepared after the deposition of Zr-IGZO film. Subsequently, a patterned 25-nm-thick Al-doped ZnO (AZO) contact buffer layer and a 200-nm-thick Titanium (Ti) metal were deposited to form source and drain (S/D) contacts. The width-to-length ratio of all the device fabrication are 200 μm /20 μm . Finally, a 200-nm-thick SiO₂ was deposited as a passivation layer by RF sputtering.

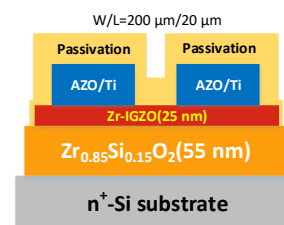


Fig. 1. Schematic of the co-sputtered Zr-IGZO TFTs with $\text{Zr}_{0.85}\text{Si}_{0.15}\text{O}_2$ gate dielectric.

3. Results and Discussion

Figure 2 shows the transfer characteristics of Zr-IGZO TFTs without and with PDA at a drain-to-source voltage V_{DS} of 4 V. A significant improvement in device performance is observed for the TFTs with a suitable Zr incorporation of about 2% on IGZO. Effect of PDA (for 10 min in N₂ at 300 °C) on the device performance is also evident.

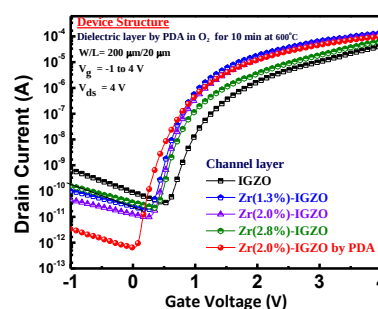


Fig. 2. The transfer characteristics of Zr-IGZO TFTs without and with PDA at a drain-to-source voltage V_{DS} of 4 V.

Based on X-ray photoelectron spectroscopy (XPS) analyses to examine the chemical bonding states, the binding energy of the O 1s peaks of Zr-IGZO films are shown in Fig. Table I summarizes the corresponding quantitative details. It reveals that the amount of oxygen vacancies are decreased after Zr incorporation because Zr^{4+} cation has a higher ionic valence and stronger oxygen affinity, as a result, density of oxygen vacancy could be suppressed [5]. As shown in Figs. 3(a)-3(e), it indicates that the $O_{\text{vac}}/(O_{\text{vac}}+O_{\text{OH}}+O)$ area ratio is decreased from 50.24 % to 38.89 %, 32.63 %, 42.17 %, and 27.46 %, respectively. Zr content in these dielectrics are estimated to be 0%, 1.3%, 2.0%, and 2.8%, respectively. TFTs with such dielectric layers are called sample A, B, C, and D sample, respectively.

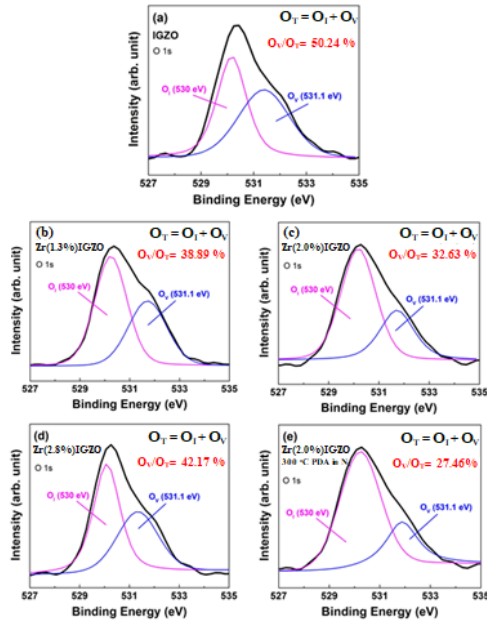


Fig. 3. X-ray photoelectron spectra of O 1s peaks for Zr-IGZO thin films.

Both positive and negative gate bias stress (at ± 4 V), short for PGBS and NGBS, were carried out to examine the effect of Zr incorporation in channel layer on the reliability of TFTs. Various stress times of 0, 10, 100, 1000 s were used. The dependence of threshold voltage shift (ΔV_{TH}) as a function of the stress time is shown Fig. 4. It shows that a positive (negative) ΔV_{TH} which increases with increasing the stress time after PGBS (NGBS). It could be due to electron trapping (detrapping) in dielectric and/or at dielectric/channel interface. Note that the magnitude of the ΔV_{TH} of NGBS is relatively less than ΔV_{TH} of PGBS because electron trapping rate is larger than the detrapping rate. Note that Zr (2.0%)-IGZO shows the best reliability among all tested samples. Figure 5 illustrates the typical transfer characteristics of Zr (2.0 %)-IGZO TFT under PGBS and NGBS. A ΔV_{TH} as low as 0.48 V and -0.34 V for PGBS and NGBS, respectively, is obtained.

Table I Zr content and oxygen vacancy in Zr-IGZO films prepared with different co-sputtering power ratios.

Sample	Power ratio: IGZO(W):ZrO ₂ (W)	Zr/(Zr+In+Ga+Zn) (%)	Symbol	Ov ac/(O _{vac} +O _{OH} +O) (%)
A	80:0	0	IGZO	50.24
B	80:30	1.3	Zr(1.3%)-IGZO	38.89
C	80:50	2.0	Zr(2.0%)-IGZO	32.63
D	80:80	2.8	Zr(2.8%)-IGZO	42.17
E	80:50	2.0	Zr(2.0%)-IGZO (300 °C PDA in N ₂)	27.46

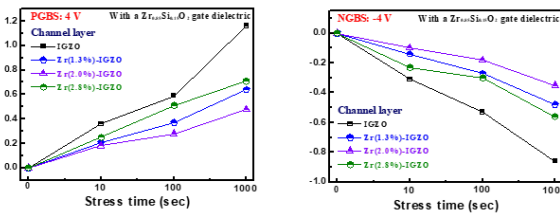


Fig. 4. Experimental ΔV_{TH} as a function of stress time for the prepared TFTs.

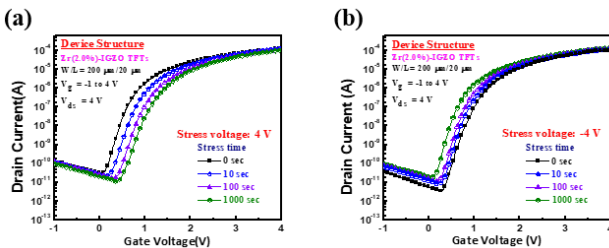


Fig. 5. Effect of stress time on Zr (2.0 %)-IGZO TFT transfer characteristics. (a) PGBS and (b) NGBS.

Effect of PDA on the device performance of Zr-IGZO TFTs is also investigated. Figure 6 shows the transfer characteristics of Zr (2.0%)-IGZO TFT with PDA in N₂ at 300 °C for 10 min after different stress times. As compared with results shown in Fig. 5, ΔV_{TH} is suppressed by about 0.105 V in average after PDA because of reduced trap density in the Zr-IGZO channel.

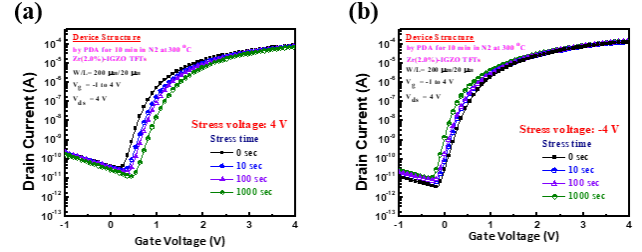


Fig. 6. Zr(2.0 %)-IGZO TFT transfer characteristics with PDA in N₂ at 300 °C after (a) PGBS (b) NGBS under different stress times.

A comparison of device electrical parameters for all the samples prepared in this work is summarized in Table II. Note that an on/off current ratio as high as 1.59×10^8 is obtained from the sample E. With Zr incorporation and a suitable PDA, interface trapped density D_{it} is seen decreasing from 3.3×10^{12} to $1.31 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$. The suppression in D_{it} is responsible for the improved SS and μ_{FE} of TFTs. Though oxygen vacancies for Zr-IGZO channel is decreased significantly after Zr incorporation, samples B and D which are with 1.3 and 2.8 % Zr content, respectively, show a higher D_{it} than that of sample C (with 2.0 % Zr content). It might be due to the channel/dielectric interface is vulnerable to plasma damage with a high co-sputtering power during Zr(2.8%)-IGZO channel deposition process [8]. Accordingly, the trade-off between the decrease in D_{it} and increase in plasma-related damage through increase the sputtering power, for power of the ZrO₂ target should be used appropriately. Our experimental results suggests that Zr incorporation in α -IGZO channel could reduce not only the density of bulk defects but also improve the device stability for improving the quality of interface with dielectric. In addition, Zr content of around 2.0% could lead to device with the best performance in switching and reliability.

Table II Electrical parameters of samples prepared in this study.

Sample	I_{on}/I_{off}	V_{TH} (V)	SS (mV/dec)	μ_{FE} (cm ² /V·s)	D_{it} (cm ⁻² eV ⁻¹)	ΔV_{TH} (V)
A	1.17×10^6	0.97	150	9.2	3.3×10^{12}	1.16
B	7×10^6	0.63	118	15.8	2.12×10^{12}	0.64
C	1.3×10^7	0.67	102	16.6	1.53×10^{12}	0.48
D	2.83×10^6	0.73	120	12.3	2.2×10^{12}	0.71
E	1.59×10^8	0.56	96	16.8	1.31×10^{12}	0.36
[9]	3.6×10^6	3.9	252	9.3	-	-1.1
[10]	7.5×10^6	3.86	110	9.8	3.83×10^{12}	0.42

4. Conclusions

In summary, improved reliability of Zr-IGZO TFTs using a co-sputtering of IGZO and ZrO₂ target in Ar plasma at RT has been demonstrate. It show that the Zr (2.0 %)-IGZO channel could provide a significant improvement in device reliability with reduced threshold voltage shift from 1.16 V to 0.36 V after PGBS for 1000 seconds and from -0.86 V to -0.23 V after NGBS for 1000 seconds. The origin of the improvement was attributable to the suppression of bulk oxygen vacancy formation after Zr incorporation in IGZO channel as confirmed by XPS analysis.

Acknowledgements

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References

- [1] M. Kimura et al., Appl. Phys. Lett. 96, 262105 (2010).
- [2] K. Takechi et al., Jpn. J. Appl. Phys. 48, 011301 (2009).
- [3] J. H. Chung et al., Thin Solid Films. 516, 5597 (2008).
- [4] J. S. Na et al., Jpn. J. Appl. Phys. 53, 03CD02 (2014).
- [5] Y. Jung et al., J. Mater. Chem. 22, 5390 (2012).
- [6] J. S. Park et al., Appl. Phys. Lett. 92, 072104 (2008).
- [7] C. H. Hung et al., Jpn. J. Appl. Phys. 56, 04CG06 (2017).
- [8] M. Kim et al., Appl. Phys. Express 90, 212114 (2007).
- [9] X. D. Huang et al., IEEE Electron Device Lett. 38, 576 (2017).
- [10] S. Y. Sung et al., Appl. Phys. Express 96, 102107, (2010).