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Doping-Less 1T-DRAM with Schottky Barrier Contact for Low Power Application

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Abstract

This work demonstrates a novel structure of Doping-Less 1T-DRAM with the schottky contact concept (not charge plasma concept). The device does not have any physical doping. It is expected to be free from problems associated with random dopant fluctuations. The source and drain regions are formed by using appropriate work functions for the source and drain metal electrodes. We use Sentaurus TCAD tools to design. Our results show that the performance of programming window is 28.71 μA/um at gate length of 10 nm. The retention time can achieve 466 ms at 300K and 79 ms at 358K. Operating bias of performance can reach 4 ns in programming time.

1. Introduction

Recently, the device follows up the limit of MOSFET scaling, decreasing the feature size is no longer mainly development. External parasitic resistance has become one of the important issues for nanometer device scaling. The SD contact resistance is conventionally minimized by heavy ion implantation. The heavy dopants result in high electric field and short depletion width in the semiconductor at the MS interface [1]. However, implantation may cause other process challenges, such as random dopant fluctuation and high thermal budgets for dopant activation [2-5]. Therefore, this structure uses MS interface schottky barrier to form N^+ region of Source and Drain. The schottky barrier uses mechanism of thermionic emission [6] that generates more electrons. The schottky barrier contact results in an efficient SB modulation in comparison with the conventional 1T-DRAM and significantly improves the performance [7-10]. We believe that our results may provide the incentive for further exploration of the Doping-Less 1T-DRAM.

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2. Results and Discussion

Our structure of Doping-Less 1T-DRAM does not have any physical doping. The silicon film thickness (T_{si}) is 20 nm, buried oxide thickness (T_{Box}) is 30 nm and oxide thickness (T_{ox}) of 3 nm is used with SiO_2 as the dielectric layer. The gate length is 10 nm as shown in Fig. 1. The Models used for the evaluation include Shockley-Read-Hall recombination and auger recombination being used to calculate retention time. Avalanche effect is considered in the carriers that will be accelerated by electric field to impact lattice. High field saturation mobility is through hydrodynamic model in the simulation. We use hydrodynamic and avalanche model to simulate impact ionization condition for the device.

We observe I_D-V_G Characteristics for different height T_p of raised body as shown in Fig. 3, which demonstrates the influence of T_p on the input characteristics. When T_p is higher, much more holes are not affected by the recombination of electrons at storage so that the current is increased. To enlarge device's programming window, we select the optimum T_p as 40 nm.

Fig. 4 shows the visible kink effect [11-12] for different of T_P. Kink effect reflects that drain current increases rapidly due to holes accumulation along with the shift in threshold voltage. Changing the height of the raised body from 50 nm to 0 nm, the enhancement of kink effect can be clearly seen. It indicates that larger TP has enough volume for impact ionization to write holes into the storage region.

Fig. 4 shows the programming window and retention time as function of the variation of T_p at 300K. The programming window and retention time are decreased if T_P is too short. The reason is that the storage holes are too close the current flow while reading and holes will be recombines rapidly. If T_P is too high, it will reduce the electric field enhancing and cause programming window decreasing.

As shown in Fig. 5 and Fig. 6, reducing hold voltage can achieve low power and low voltage operation for IoT application. And we also tried to change V_g bias from -1 V to - 0.4 V, current of read '1' reaches saturation after V_g bias of - 0.4 V. Performance of programming window and retention time were attained steadily.

Currently, there are many kinds of metal materials, which can demonstrate our result in the experiment. We are going to study the impact of work functions with equivalent oxide thickness (EOT) 1 nm as shown in Fig. 7. In Fig. 7, we can observe material of Al (4.06 eV) which exhibits maximum programming window.

We also attempt to use different operating drain bias to realize power consumption's issue. Fig. 8 shows power consumption for four operating state. The main factor to influence retention time is the recombination rate. At the programming state, biasing drain voltage 1.0 (V) can save 28.7 % power consumption compared to that of biasing drain voltage 1.2 (V). Besides, the erasing state without biasing drain voltage can save large power consumption.

As shown in Fig. 9, we simulated DL 1T-DRAM, which V_g is -1 V and V_d is 1 V in 300K. We applied different T_P for the simulation and we can observe that programming time 4 ns is achieved. If voltage of drain is large than 1.1 V, the programming time can below 3 ns. If we want to do a low power supply operation, such as drain voltage (V_d) of Write'1' can be low to 0.9 V. This DL 1T-DRAM, thus, can be applied for IoT application in the nearest future.

3. Conclusion

This work has demonstrated a Doping-less 1T-DRAM with the schottky contact for low power application. In-depth analysis of Doping-less 1T-DRAM demonstrates that through appropriate use of suitable metal materials (with suitable work functions values), the good performance can be achieved. Our results show that the performance of programming window 28.71 μA/um at the gate length of 10 nm can be achieved, and retention time can achieve 466 ms at 300K and 79 ms at 358K as well. Besides, the programming time can reach 4 ns. This work

provides a new approach to understand the structure of the Doping-less 1T-DRAM for IoT use in the nearest future.

Acknowledgments

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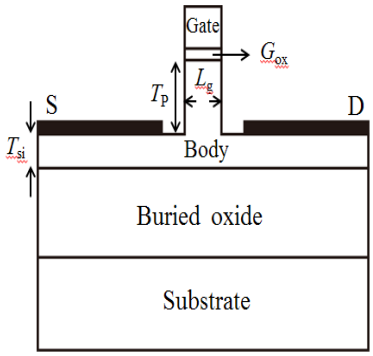

Fig. 1. The structure of Doping-less 1T-DRAM with suitable work function material for source and drain electrodes. The hole can store in the raised body.

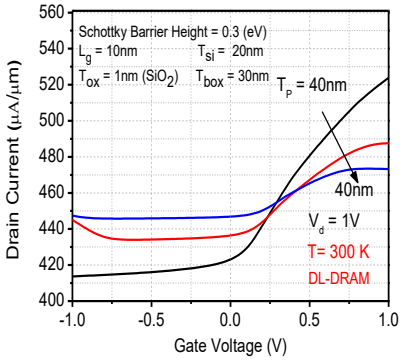

Fig. 2. I_D-V_G Characteristics for different T_p. We demonstrate that T_p will influence gate controllability.

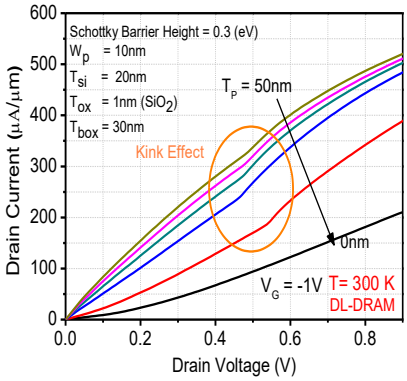

Fig. 3. I_D-V_D Characteristics of different thickness of body. It can be clearly seen that kink effect occurs on the curve.

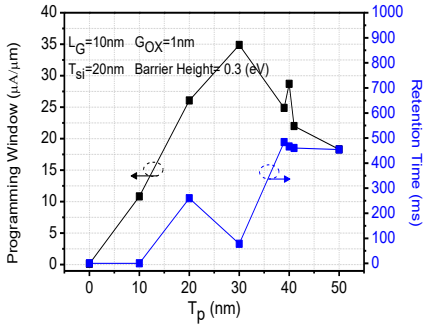

Fig. 4. The programming window and retention time versus the variation of T_p at 300K.The better performance is derived as T_p = 40nm.

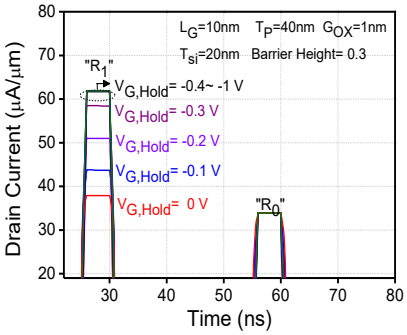

Fig. 5. Drain currents and programming window versus different hold biases.

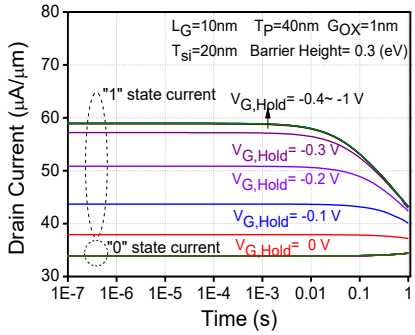

Fig. 6. Retention time versus different hold biases.

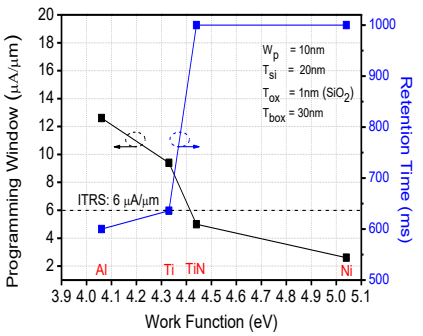

Fig. 7. Programming window and retention time of different Metal materials of source and drain contacts.

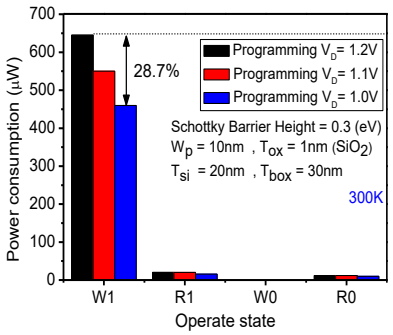

Fig. 8. Power consumption of different DRAM operating state for different drain bias.

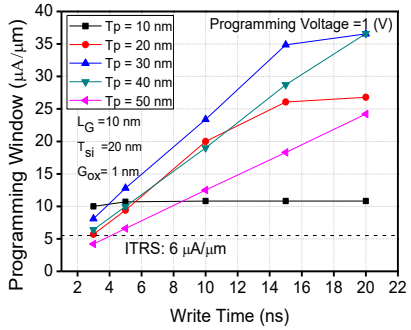

Fig. 9. Programming window versus write time under different T_P.