Extended Abstracts of the 2018 International Conference on Solid State Devices and Materials, Tokyo, 2018, pp907-908

Vertical Double Gate Transistor with N-Bridge for Low Power 1T-DRAM

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Abstract

In this paper, we propose a vertical Double Gate transistor with N-Bridge DRAM (VN-DRAM) for low power applications. The vertical channel of the device can reduce short channel effects and improve scalability. Conventional current bridge device only has one side gate-controlled depletion region but the proposed VN-DRAM has double gate-control depletion region which can improve programming window (PW) at short gate lengths.

1. Introduction

Memory devices are essential for the successful implementation of Internet of Things (IoT) as new devices are required more than ever to deal with the processing, power consumption, cost and speed demands [1]. The memory devices with high integration density are not only needed to improve its performance, but also to operate with low power. DRAM is a very useful component for IoT applications [2]. However, Conventional DRAM's capacitor requires a complicated process and additional space to obtain sufficient storage capacitance. 1T-DRAM is proposed to resolve the conventional DRAM problem [4-11].

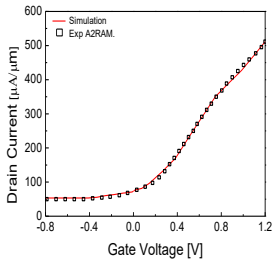
Raised Body 1T-DRAM [5] and Trench 1T-DRAM [6] are the floating-body based devices, but it needs long programming time and large power supply. GaP S/D 1T-DRAM [7] has excellent retention time up to 900 ms, but the device needs excellent quality of interface between GaP and silicon surface. TFET 1T-DRAM [8-9] is a new kind of memory. This kind of 1T-DRAM has good retention time. However, its programming window only reaches 500 nA. It might be too small to use.

ARAM [10] possesses a structure of a storing body and an N^+ doped current bridge. It has also good retention time up to 100 ms at 300K. A2RAM [11] is a competitive memory device which has simple process and good memory performance. However, it needs high operating biases and its gate can't be self-aligned.

2. Results and Discussion

It is analyzed by using the well calibrated models with experimental data [11] as shown in Fig. 1. Fig. 2 shows the structure of VN-DRAM. The structure has P doped storage region with concentration of 10^{15} (cm^{-3}) and n^+ doped channel region with 10^{18} (cm^{-3}).The gate length is 10 (nm). In the write'1' operation, the device uses Gate-induced-drain-leakage (GIDL) to generate holes in the twin p-body. In the write'0' operation, a positive voltage is applied to gate to exclude holes from the store region.

Fig. 3 shows VN-DRAM's reading state mechanism. During read "1" operation, the gate electric field emitted from negative gate bias is screened by the positive hole charges of the p-body and has a minor effect on the majority carriers of the n-Bridge. As shown in Fig. 3 (a). When p-body lacks holes, the gate field is no longer screened and the depletion region will be induced and expanded along the n-bridge. Thus, the current path will exhibit less current flow from drain to source (Fig. 3b).



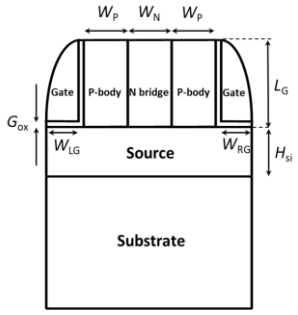


Fig. 1 Comparison I_D-V_G with exp. [11]. Fig. 2 Schematic of VN-DRAM cell.

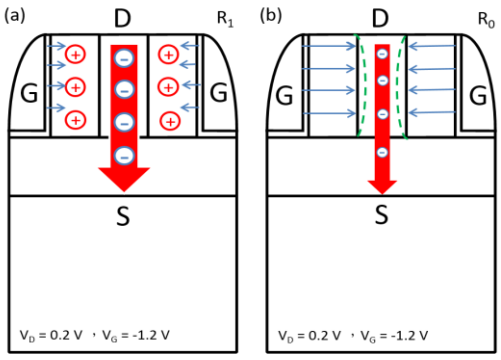


Fig. 3 Schematic operation of VN-DRAM cell. (a) Reading '1' state: increasing drain bias leads to current flow. (b) Reading 0 state: current flow being reduced to zero.

Fig. 4 shows the kink effect is visible at voltage V_G = -0.8 V to V_G = -1.5 V. Kink effect reflects that drain current increases rapidly due to the threshold voltage shift due to hole accumulation. When the kink effect is more obvious, it indicates greater accumulation of holes in the storage region.

Fig. 5 shows the Programming window versus write time at different voltages at 358 K, where writing time is varied

from 3 ns to 20 ns. It can be observed that at drain voltage 1.3 V it has larger drain current, so it can be operated in writing time = 4 ns. At drain voltage 1.1 V, although the write time is around 9 ns, it is still less than 10 ns and at lower applied voltage.

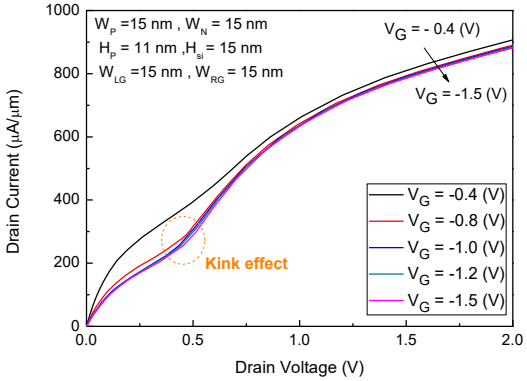


Figure. 4. $I_D - V_D$ Characteristic curve at different voltages.

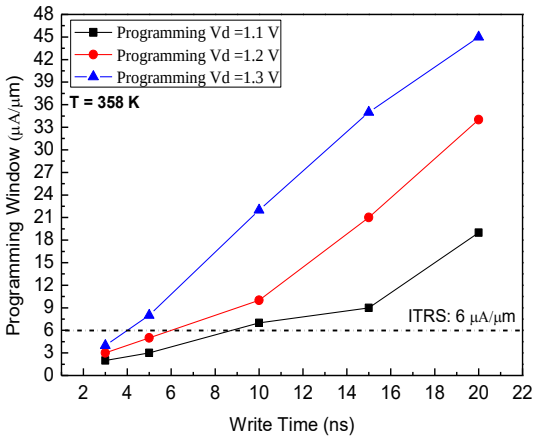


Figure. 5. Programming window versus Write time with different voltages of VN-DRAM at 358 K.

We attempt to use different operating drain voltage to overcome the power consumption issue. Fig. 6 shows the power consumption at four operating states. In the programming state, biasing drain voltage 1.0 V can save 32.5 % compare to 1.2 V. Besides, the erasing state without biasing drain voltage can save power consumption.

3. Conclusion

In this paper, we have proposed a vertical double gate transistor with n-bridge for low power 1T-DRAM. This VN-DRAM has better scalability compared with the planar device. The retention time is 360 ms and the programming window remains 36 μA/μm which is useful for lower technology nodes. VN-DRAM has high speed operation which can reach 6 ns for Write '1' operation. When operated at power supply 1 V, it can reduce 32.5% power consumption for Write'1' compared to that of power supply 1.2 V. All biases of VN-DRAM are lower than 1.2 V while operating.

Then, we make the Fig. 7 for programing window and retention time comparison more clearly. As shown in Fig. 7, our device has large programing window and long retention time. Another important thing is the device's operating voltage. Some memory device has high performance, but it caused too much power consumption.

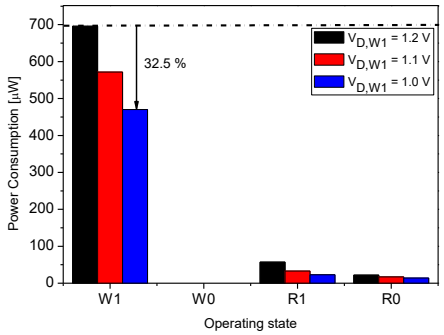


Figure. 6. The power consumption with different operating drain voltage.

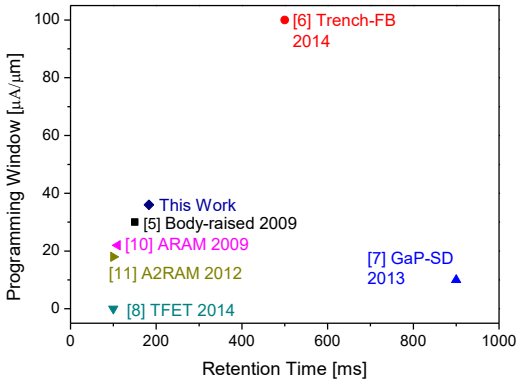


Fig. 7. The 1T-DRAM comparison with retention time and programing window.

Acknowledgments

This work was supported by National Science Council (MOST-104-2923-E-110-001-MY3), National Center for High-Performance Computing (NCHC) of National Applied Research Laboratories (NARLabs), National Nano Device Laboratories (NDL) of Taiwan, and by Department of Science and Technology, Government of India, through Global Innovation and Technology Alliance (GITA) under Grant No. GITA/DST/TWN/P-70/2015.

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