Extended Abstracts of the 2018 International Conference on Solid State Devices and Materials, Tokyo, 2018, pp909-910

Memory characteristics of band modulated FET on nano SOI

Sehyun Kwon[1,2], Jinho Ahn[*2], Sorin Cristoloveanu[3], Francisco Gamiz[4], Carlos Navarro[4], Philippe Galy[5]
Young Min Jhon[1], and Yong Tae Kim[*1]

[1] Korea Institute of Sciences and Technology, Seoul 02792, Korea
[2] Hanyang University, Seoul 04763, Korea
3IMEP-LAHC, Grenoble INP Minatec, Grenoble, France
[4]University of Granada, Granada, Spain
[5]STMicroelectronics, Grenoble, France
E-mail: ytkim@kist.re.kr, jhahn@hanyang.ac.kr

Abstract

Band modulated field effect transistor (FET) on nano silicon on insulator (SOI) has been suggested for memory application. DC and AC operation mechanisms are investigated with potential profiles and electron-hole concentrations in channel region. The devices show nealy zero subthreshold swing and memory operations by read/write of '0' and '1' states with retention time of 1.8s..

1. Introduction

For Internet of Everything (IoE) application, emerging memory technology requires low power consumption and capacitor-less scalability with standard CMOS process. In this work, we have suggested band modulated FET on nano SOI as a capacitor-less 1 transistor-DRAM. The FETs are fabricated with 28nm node technology and the device structure is described in Fig. 1. Undoped floating Si body (T_{Si}) is 7nm and thickness of buried oxide (T_{BOX}) is 25nm. Dual gates consist of a control gate (L_G) and another ungated channel (L_{int}), and L_G and L_{int} are 200 and 200nm, respectively. Anode (A) and cathode (K) contact with P^+ and N^+ type Si epi-layers and back gate (G_B) is applied to back side polysilicon layer (GP-P).

2. DC characteristics and simulation

The I-V curve was measured by forward and backward anode voltage (V_A) sweeping from 0V to 2V with various front gate voltages (V_{Gf}) from 0.6 to 1.2V as shown in Fig. 2. At off regime, current is very low until the turn on voltage (V_{ON}) triggers barrier collapsing state. At the barrier collapsing region sharp turn on occurs since the injection barrier at the anode side is lowered by forward V_A and V_{Gf}, the hole carriers are injected into the channel region without any impact ionization due to very thin and fully depleted silicon body [1, 2]. These hole carriers from A to K reduce the electron injection barrier and electrons flow from K to A. This band modulation provides nearly zero swing slope, zero impact ionization, and '1' state with very high on/off current ratio of over 10^7. At '1' state, the front gate and back gate bias stores the electrons and holes in the body. When V_A decreases to 0V the device will switch off and behaves as a PIN diode in on-state

DC characteristics are analyzed by Synopsis TCAD 2D simulations to study the evolution of potential and carrier

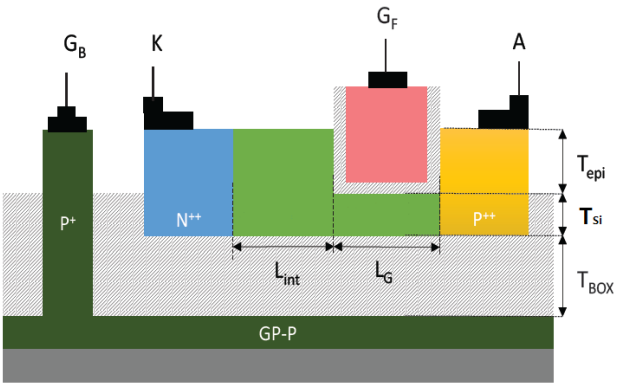

Fig. 1. Structure of modulated FET on 7nm SOI

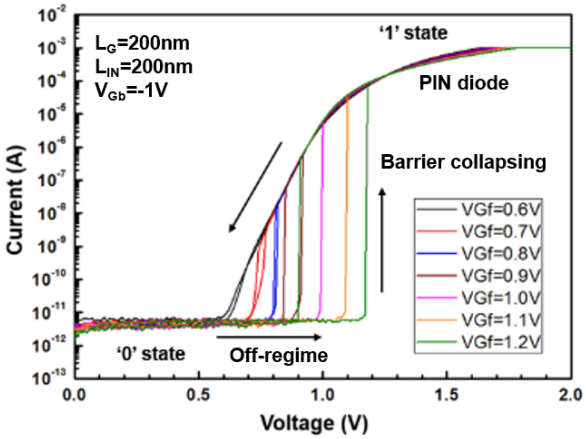

Fig. 2. DC characteristics of modulated FET on 7nm SOI

densities corresponding to off, barrier collapsing, and PIN diode regimes. In the off region, Fig. 3 (a) shows that when V_A increases the potential in the gated region increases, and electron density (n) decreases until its value is close to intrinsic concentration (ni). In addition, hole density (p) increases in gated region that enables to keep $np \sim ni^2$. This means that PN junctions in the channel region stay unpolarized and anode current is very slightly increased with V_A during off region. In Fig. 3 (b), the barriers collapsing regime, the potential in the gated region has reached its maximum value and n in ungated region is equal to p in the gated region, which results in polarized PN junctions and directly sharp switching since strong anode current increase. Fig. 3 (c) indicates PIN diode regime, the potential increases first only in ungated

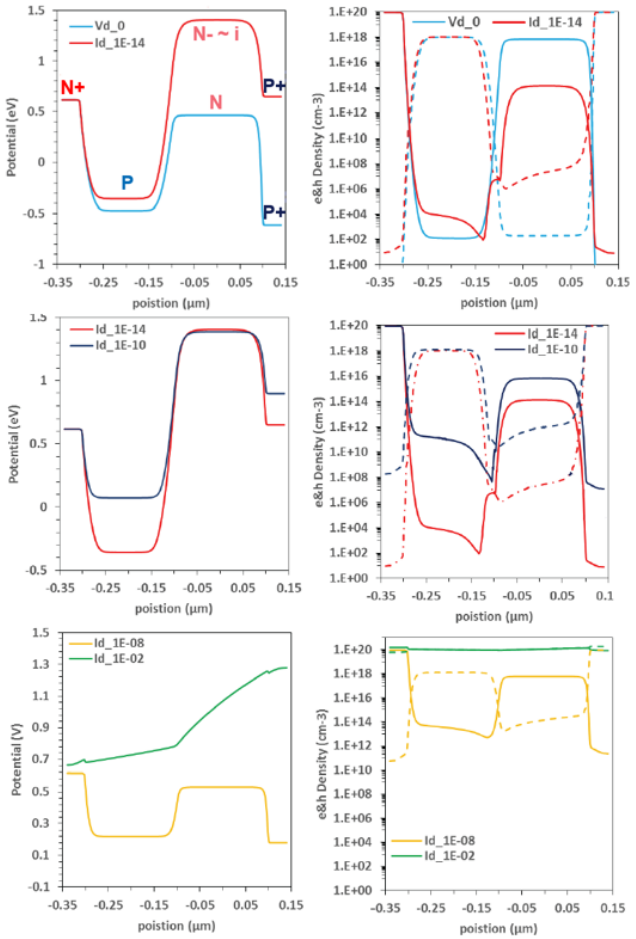

Fig. 3. Evolution of potential, electron and hole densities corresponding to off, barrier collapsing, and PIN diode regimes (solid line represents n and dot line represents p)

region, leading to no potential barrier between the gated and ungated regions. It is similar to standard PIN diode potential variation, and n/p increase in both regions. As a consequence, the anode current saturates for high V_A because of the intrinsic resistance of the SOI.

3. Memory characteristics and discussion

To investigate the memory transient operations, Write‘0’-Read-Write‘1’-Read (W0-R-W1-R) pulses are applied as shown in Fig. 4, and potential and carrier concentrations are analyzed. During write ‘0’, V_{Gf} is lowered to 0V which lowers the potential barrier under the front gate. The accumulated electrons under the front gate are eliminated within the channel by moving to the anode due to lowered potential barrier which can be seen through decreasing electron concentration on the gated region. When reading ‘0’ state, V_A is increased to 1V and the potential barrier slightly decreases with no significant change in carrier concentration. Thus, very low current is observed in this state. As the V_{Gf} drops to 0V and the V_A rises to 1V, the potential barrier is lowered and the carriers at anode and cathode are injected into the channel making ‘1’ state. The carrier concentration in the channel is very high at

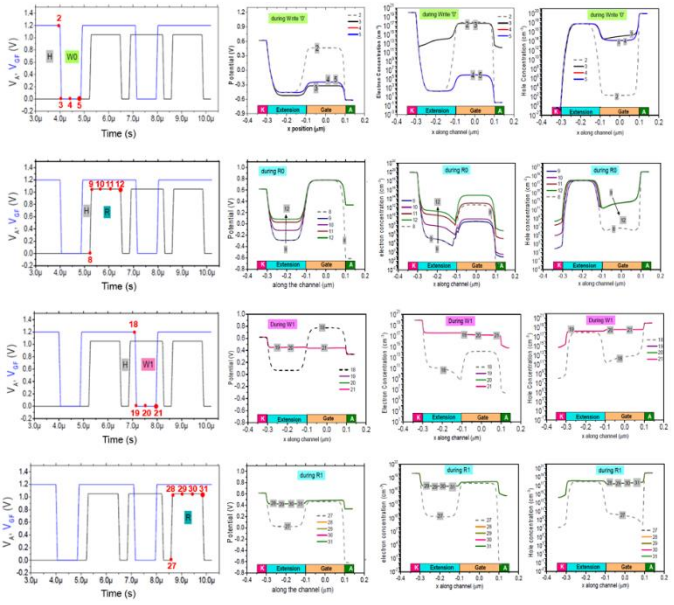

Fig. 4. Potential and carrier densities during (a) write’0’, (b) read’0’, (c) write’1’, and (d) read’1’operations

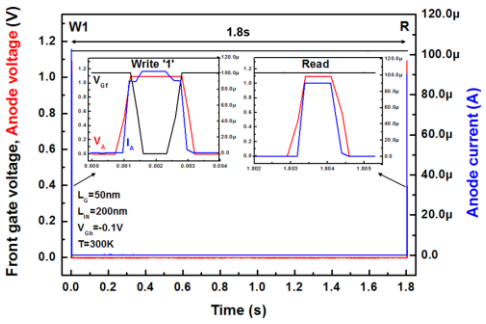

Fig. 5. Retention time of ‘1’ state

this state hence when reading ‘1’ state, the potential barrier at each side is flattened and high current is observed. How long the current remains low at ‘0’ state and high at ‘1’ state is determined by retention time. Fig. 5 shows that the current of ‘1’ state remains high even after 1.8s.

4. Conclusion

The band modulated FETs are fabricated, and electrical characteristics are measured and analyzed with 2D TCAD simulation. As a result, the devices show nearly zero swing slope and very high on/off current ratio. The memory transient characteristics also show successful W0-R-W1-R operations with long retention time of 1.8s at ‘1’ state.

5. Acknowledgements

This research is supported by National Research Foundation under the Grant No.2016M4A7B4024131.

References

[1] Y.T. Kim et al, IEEE, Trans. Electron Devices, **64**, 2 (2017) 4904

[2] Y.T. Kim et al, Conf. on *Euro SOI*, 19-31 March, Granada, Spain (2018)