

Device Size Dependence of Hf-based MONOS Nonvolatile Memory for Multi-level 2-bit/cell Operation

Sohya Kudoh¹, and Shun-ichiro Ohmi²

Department of Electrical and Electronic Engineering, Tokyo Institute of Technology
J2-72, 4259 Nagatsuta, Midori-ku, Yokohama 226-8502, Japan

Phone: +81-45-924-5481 E-mail: kudoh.s.ab@m.titech.ac.jp¹, ohmi@ee.e.titech.ac.jp²

Abstract

This paper investigated the device size dependence of Hf-based Metal-Oxide-Nitride-Oxide-Silicon (MONOS) nonvolatile memory (NVM) for the 2-bit/cell operation. It was found that 2-bit/cell operation was realized with the device of gate length (L) and width (W) = 2 - 10/15 - 90 μm . Furthermore, it was realized that electron injection from drain region affected I_D - V_G transfer characteristics at V_{TH} even for $L/W = 2/90 \mu\text{m}$.

1. Introduction

Recently, the charge trapping (CT) type NVM such as MONOS has been attracted much attention [1,2]. Furthermore, 2-bit/cell operation was necessary to achieve the high integration [3,4]. It was found that Hf-based MONOS NVM was able to realize 2-bit/cell operation by changing the electron injection region from source region to drain region [5]. Furthermore, it is necessary to investigate the effect of injected electron from each region on the drain current characteristics to improve 2-bit/cell characteristics.

In this paper, 2-bit/cell characteristics dependence on device size for Hf-based MONOS NVM were investigated.

2. Experimental Procedure

The Hf-based MONOS NVM was fabricated on p-Si(100) substrate using the typical gate-last process [2]. After the channel stop ion implantation and the local oxidation of silicon (LOCOS) isolation, source and drain (S/D) ion implantation was carried out. Then, the $\text{HfN}_{0.5}/\text{HfO}_2/\text{HfN}_{1.0}/\text{HfO}_2$ (MONO) structure with thickness of 10/10/3/2 nm respectively, was in-situ deposited by ECR plasma sputtering at room temperature (RT) [2]. Then, post-deposition annealing (PDA) was carried out at 600°C/1 min in N_2 of 1 SLM. Next, the contact hole was formed by reactive ion etching (RIE) with Ar/ Cl_2 of 50/20 sccm [2]. After the Al electrode was evaporated and patterned to form pad electrode, the $\text{HfN}_{0.5}$ metal layer was etched by DHF. After Al back electrode was evaporated, post-metallization annealing (PMA) was carried out at 300°C/10 min in $\text{N}_2/4.9\%\text{H}_2$ at 1 SLM. The gate length (L) and width (W) were $L/W = 2 - 10/15 - 90 \mu\text{m}$. Figures 1 (a) and 1 (b) show the schematic cross-section and the plane-view of Hf-based MONOS NVM [2].

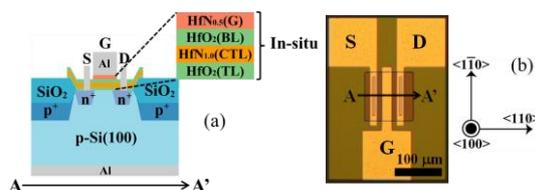


Fig. 1 (a) Schematic cross-section (A-A') of Hf-based MONOS NVM and (b) plane-view [2].

The electrical characteristics of NVM were evaluated by I_D - V_G . The operation conditions were set as $V_{\text{PGM}}/t_{\text{PGM}}$ of 6 V/2 ms, $V_{\text{ERS}}/t_{\text{ERS}}$ of -10 V/1 s and V_{DS} of 1.5 - 5 V. All measurements were carried out at RT in air.

3. Results and Discussion

Figure 2 shows the schematic description of 4 states for Hf-based MONOS NVM when the operation conditions were set as $V_{\text{PGM}}/t_{\text{PGM}}$ of 6 V/2 ms, V_{D} (V_{S}) of 1.5 - 5 V and V_{S} (V_{D}) of 0 V, which injected the electron from the source (drain) region. Figure 3 (a) shows the I_D - V_G characteristics of "11" and "01" states with changing the read direction. Figures 3 (b) and 3 (c) show the schematics of forward read and reverse read operation of each "01" state, respectively. The forward (reverse) read operation condition was set as V_{D} (V_{S}) of 1.5 V and V_{S} (V_{D}) of 0 V. It was found that I_D - V_G transfer characteristics were not affected by read direction.

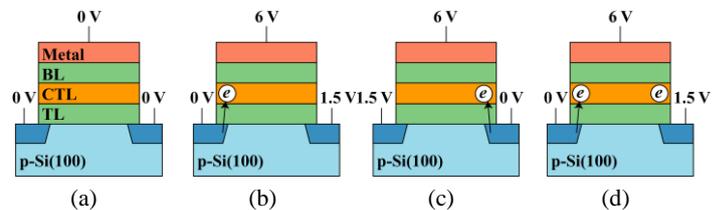


Fig. 2 Schematic 4 states of Hf-based MONOS NVM [5]. The states of (a) "11", (b) "10", (c) "01" and (d) "00".

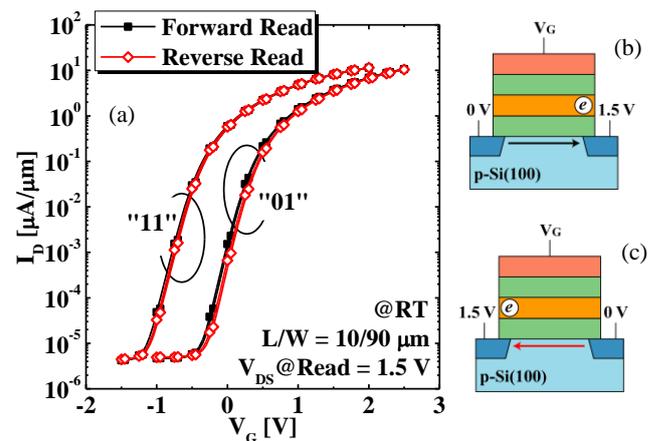


Fig. 3 (a) I_D - V_G characteristics of "11" and "01" states. $V_{\text{PGM}}/t_{\text{PGM}}$ was 6 V/2 ms and V_{DS} was 1.5 V at the program and read operation. (b) Schematics of forward read operation and (c) reverse read operation of "01" state.

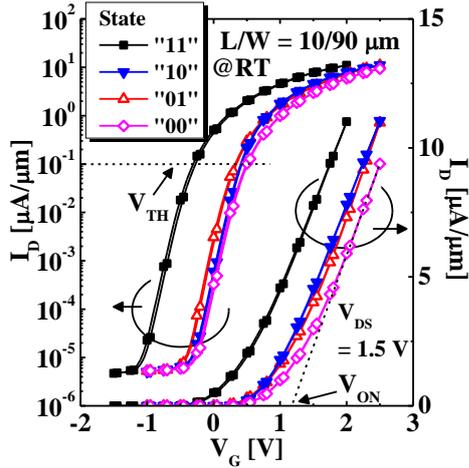


Fig. 4 I_D - V_G characteristics of 4 states. V_{PGM}/V_{DGM} was 6 V/2 ms and V_{DS} was 1.5 V at the program. V_{DS} was 1.5 V at the forward read operation.

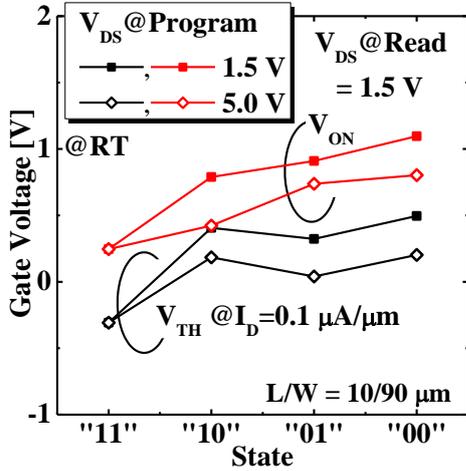


Fig. 5 V_{ON} and V_{TH} at each state. Open symbol denoted V_{DS} of 5 V at program operation. V_{DS} was 1.5 V at the forward read operation.

Figure 4 shows the I_D - V_G characteristics of 4 states with changing the electron injection region. Here, the V_{ON} and V_{TH} were defined as the V_G intercept of the linear extrapolation of the I_D - V_G characteristics and the V_G at I_D of 0.1 $\mu\text{A}/\mu\text{m}$, respectively. Figure 5 shows the V_{ON} and V_{TH} at each state extracted from I_D - V_G characteristics. V_{ON} at “10” state was 0.1 - 0.3 V smaller compared with V_{ON} at “01” state in both cases of V_{DS} of 1.5 V and 5 V at the program operation. However, V_{TH} at “10” state was 0.2 V larger than V_{TH} at “01” state. This is because I_D - V_G characteristics of “10” state at V_{TH} was steeper compare with the states at “01” and “00” as shown in Fig. 4. It was found that drain region electron injection affected I_D - V_G transfer characteristics at V_{TH} . Figures 6 (a) and 6 (b) show the gate width dependence on V_{ON} and V_{TH} , respectively. The dependence of V_{ON} and V_{TH} on “10” and “01” states were not changed with decreasing the gate width as shown in Figs. 6 (a) and 6 (b). Furthermore, Figs. 6 (c) and 6 (d) show the gate length dependence on V_{ON} and V_{TH} , respectively. The dependence of V_{ON} and V_{TH} on “10”

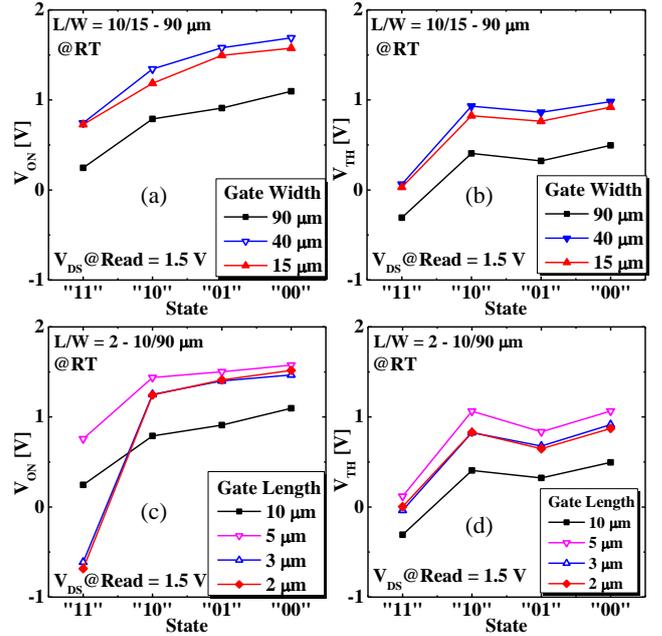


Fig. 6 Gate width dependence on (a) V_{ON} and (b) V_{TH} at each state. Device sizes were $L/W = 10/15 - 90 \mu\text{m}$. Gate length dependence on (c) V_{ON} and (d) V_{TH} at each state. Device sizes were $L/W = 2 - 10/90 \mu\text{m}$. V_{DS} was 1.5 V at the forward read operation.

and “01” states were not changed even for $L/W = 2/90 \mu\text{m}$. These results suggested that the electron injections from S/D region were able to be read independently even for short channel in the case of Hf-based MONOS NVM.

4. Conclusions

We investigated the electrical characteristics of Hf-based MONOS NVM for 2-bit/cell operation. It was found that 2-bit/cell operation was realized utilizing fabricated devices of $L/W = 2 - 10/15 - 90 \mu\text{m}$. Furthermore, electron injection from drain region affected I_D - V_G transfer characteristics at V_{TH} even for $L/W = 2/90 \mu\text{m}$. In conclusion, Hf-based MONOS NVM is one of the candidates to realize 2-bit/cell operation with scaling.

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