Extended Abstracts of the 2018 International Conference on Solid State Devices and Materials, Tokyo, 2018, pp913-914

# Effects of Si Content in $Si_3N_4/ZrO_2$ Stacked Trapping Layer on Operation Characteristics of Poly-Si Gate-All-Around Charge-Trapping Flash Memory Devices

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**Abstract**

**Operation characteristics of poly-Si gate-all-around charge-trapping flash devices with various Si contents and thicknesses in $Si_3N_4/ZrO_2$ stacked trapping layers are investigated. The operation speeds of devices with richer Si in SiN trapping layer are much faster due to more shallow traps near the tunneling oxides, which however also cause retention degradation. A slightly rich Si in SiN trapping layer is useful to improve operation speeds and keep comparable reliability characteristics of flash devices.**

## 1. Introduction

Due to the fast increasing demands of non-volatile memory market, polycrystalline silicon (poly-Si) channel has been widely applied on high density flash devices [1]. Since junction dopants in high density memory devices are difficultly formed, junctionless (JL) channel was proposed to omit junction formation by simultaneously doping source/drain (S/D) and channel into the same type. However, the slower erasing speed is a serious concern for JL charge-trapping flash devices. Recently, gate-all-around (GAA) configuration was widely applied on charge-trapping (CT) flash devices, indicating that operation characteristics can be much improved by GAA configuration[2]. The electric field enhacement provided by GAA configuration may cause the injected charges trapped near the blocking oxide, which may result in slow erasing speed. Furthermore, stacked trapping layer such as $Si_3N_4$/high-k was reported to enhance the operation speed and reliabilities of CT flash devices. Since a thicker SiN can trap more injected charges near the tunneling layer for device with GAA configuration and more Si content in SiN can provide more shallow traps [3], the stored charges can be detrapped easier during erasing operation. Thus, more Si contents in SiN and optimal thickness of SiN may be helpful to improve operation speeds of flash devices. In this work, effects of Si contents in SiN trapping layer with different thicknesses on poly-Si GAA CT flash devices are studied.

## 2. Device Fabrication

The fabrication processes of GAA active region are very similar as in [4]. After the active region formation, a 3 nm thick $SiO_2$ tunneling layer was grown on all samples by rapid thermal oxidation (RTO). Then, a 3 nm thick nitrogen rich SiN was deposited on NR30 sample, a 4 nm thick nitrogen rich SiN was deposited on NR40 one, a 4 nm thick Si rich SiN was deposited on SR one, and a 4 nm thick Si rich-

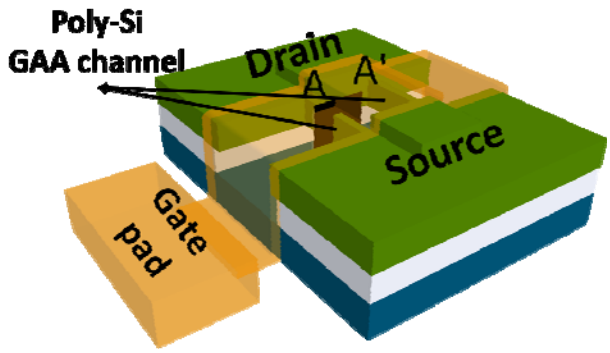


Fig. 1. Schematic diagram of poly-Si GAA CT flash device with $Si_3N_4/ZrO_2$ stacked trapping layer.

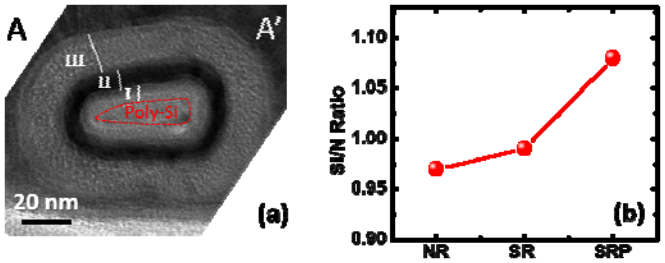


Fig. 2. (a) Cross-sectional TEM image of poly-Si GAA CT flash device with $Si_3N_4/ZrO_2$ stacked trapping layer. (b) Si/N ratios in SiN trapping layers by XPS analysis.

er SiN was deposited on SRP one by a low pressure chemical vapor deposition (LPCVD) system, respectively. Then high-k stacked trapping layer deposition, gate formation, passivation, metallization and sintering were performed as the same in [4]. The schematic diagram of poly-Si GAA CT flash device with $SiN/ZrO_2$ stacked trapping layer is shown in Fig. 1.

## 3. Results and Discussion

The cross-section TEM image of poly-Si GAA CT flash device with $Si_3N_4/ZrO_2$ stacked trapping layer is shown in Fig. 2(a). The width and height of GAA channel are about 35 and 7 nm, respectively. The thickness of $SiO_2$+SiN (I region), $ZrO_2$ high-k trapping layer (II region) and $Al_2O_3$ blocking layer (III region) are 7, 7, and 18 nm, respectively. Fig. 2(b) shows the Si/N ratio of SiN layer for NR, SR and SRP devices measured by XPS. The Si/N ratio in SRP sample increases about 10% as compared to that in NR ones. Fig.3 show initial transfer curves of all samples in this work. All devices show high on/off current ratio and small subthreshold swing. The memory windows of each device are

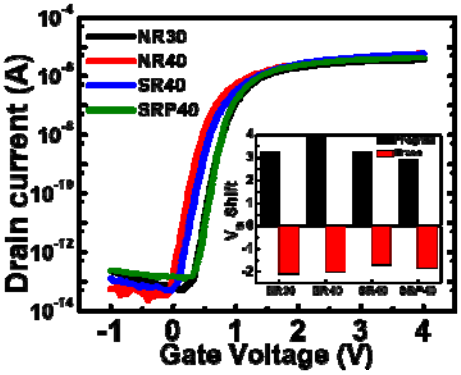


Fig. 3. Initial Id-Vg curves and memory window of poly-Si GAA CT flash devices with various SiN/$ZrO_2$ stacked trapping layers.

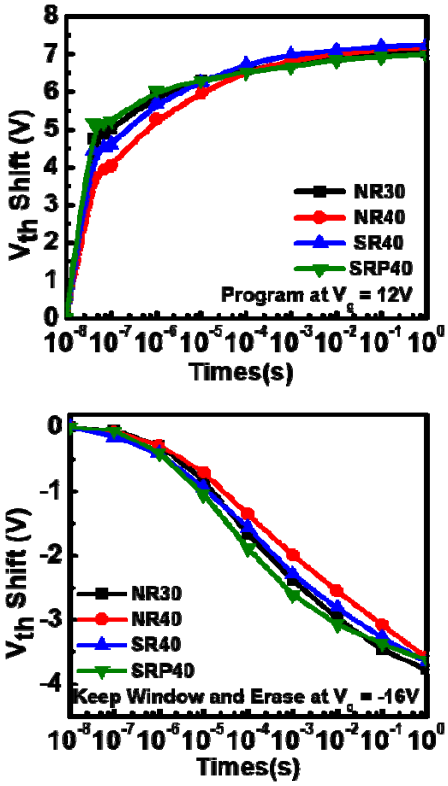


Fig. 4. (a) Programming and (b) erasing speed of poly-Si GAA CT flash devices with various SiN/$ZrO_2$ stacked trapping layers.

also shown in the inset of Fig. 3. The memory windows of samples with different thickness of SiN are similar. Fig. 4 shows (a) programming and (b) erasing speeds of all devices. SRP40 device shows the fastest programming and erasing speeds. The programming speed of NR40 is slower than that of NR30. The programming speed becomes slower when the thickness of SiN increases. A slower programming speed is caused by an increased dielectric thickness due to a smaller electric field across the tunneling layer. However, when the Si content in SiN increases, both programming and erasing speeds are improved. More charges are stored near the tunneling layer by shallow traps in SiN. Then, the charges could be captured easier during programming and be de-trapped faster during erasing operations. Fig. 5 shows retention characteristics at room temperature and 85 °C of all samples in this work. All devices show good retention

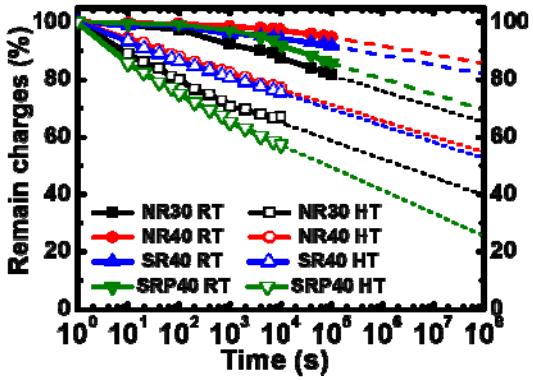


Fig. 5. Retention characteristics of poly-Si GAA CT flash devices with various SiN/$ZrO_2$ stacked trapping layers.

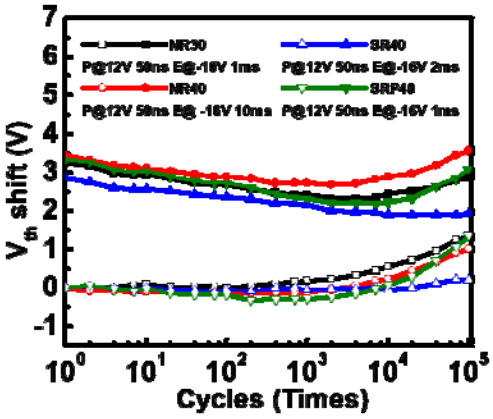


Fig. 6. Endurance characteristics of poly-Si GAA CT flash device with various SiN/$ZrO_2$ stacked trapping layers.

and remain over 70% of charges even after extrapolating the measure time to 10 years. However, SRP40 device shows the worst retention at 85 °C. More shallow traps in SiN may cause more charge loss at a higher temperature. Endurance characteristics of all devices are shown in Fig. 6. SR40 device shows the smaller window shifts as compared to the others, which may be attributed to the defects at SiN/tunneling oxide interface are fewer. Thus, a SiN tapping layer with slightly rich Si content is useful to improve reliability characteristics of flash devices.

## 3. Conclusions

Effects of Si content in $Si_3N_4$/$ZrO_2$ stacked trapping layer on operation characteristics of poly-Si GAA CT flash devices are studied. Faster operation speeds of flash device can be achieved with Si richer in SiN trapping layer, which however causes degraded reliability due to more shallow traps near tunneling oxide. A slightly rich Si in SiN tapping layer can be applied to improve operation speeds of CT flash devices, and it also maintains reliability characteristics.

## References

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