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Ge Surface Channel Formed by Different Temperature Processes on Characteristics of Poly-Si Charge-Trapping Flash Memory Devices

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Abstract

Operation characteristics of poly-Si charge-trapping flash memory devices with Ge surface channels formed by different temperatures were studied. Devices with Ge surface channel formed by high temperature process show faster program/erase speeds and better reliability. Operation speeds of devices with Ge surface channel formed by low temperature process are slower due to its thicker Ge film on poly-Si channel and incomplete Ge oxidation for forming tunneling layer.

1. Introduction

Due to the fast increasing demands of non-volatile memory market, polycrystalline silicon (poly-Si) channel has been widely applied on high density charge-trapping (CT) flash memory devices [1]. The operation speeds of CT flash memory devices can be enhanced by incorporating Ge into Si channel. A CT flash memory device with SiGe buried layer formed on poly-Si channel shows faster operation speeds owing to more carrier supply, enhanced electric field in the tunneling layer and lower tunneling barrier [2]. However, the concentration of Ge film deposited by ultra-high-vacuum chemical molecular epitaxy (UHV-CME) system at a high temperature on poly-Si is not enough. The thermal budget of fabracation proces for CT flash device should be minimized to realize 3D high density memory applications. Moreover, the undesirable Ge diffusion is more for Ge deposition at a high temperature. The Ge content in SiGeO tunneling layer near poly-Si channel should be increased since the programming and erasing (P/E) speeds of CT flash devices are influenced by the band offset of tunneling layer. A thin high quality amorphous Ge film formed with an Inductively Coupled Plasma Chemical Vapor Deposition (ICP-CVD) can provide more Ge content in tunneling oxide above the poly-Si channel. In this work, Ge surface channel formed by a low temperature deposition (ICP-CVD) and high temperature process (UHV-CME) on CT flash devices are investigated. Operation characteristics of CT flash devices with GeO_2/SiO_2 (GS) and GeO_2/Al_2O_3 (GA) stacked tunneling layer are also studied.

2. Device Fabrication

The fabrication processes of active region are very similar as in [3]. After the active region formation, a thin amorphous Ge was deposited on two of the samples by low temperature (LT) ICP system as LT-GS and LT-GA devices. Since the deposition temperature of ICP were lower, the diffusion of Ge during deposition can be limited. A thin epitaxy like layer of Ge was deposited on HT-GS and HT-GA devices by UHV-CME system at a higher temperature over 500° C. Then, the Ge on all samples were oxidized by rapid thermal oxidation. Then a SiO_2 tunneling oxide layer was deposited by ICP system on LT-GS and HT-GS devices, and an Al_2O_3 tunneling layer was deposited by an atomic layer deposition (ALD) system on LT-GA and HT-GA devices. Stacked trapping layer deposition, gate formation, passivation, metallization and standard sintering were performed as the same in [4].

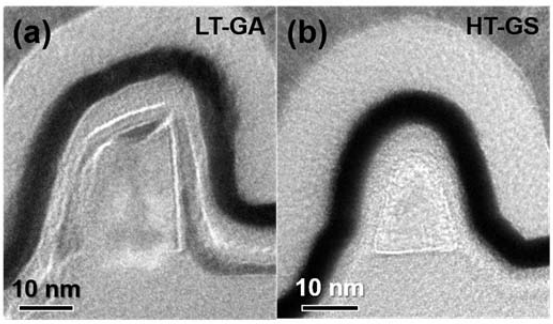

Fig. 1. Cross-sectional TEM images of (a) LT-GA and (b) HT-GS poly-Si CT flash device.

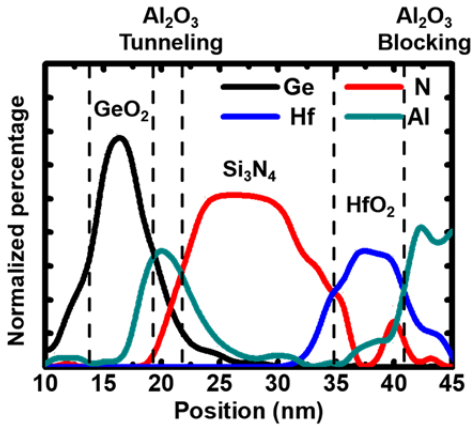

Fig. 2. EDS analysis of LT-GA poly-Si CT flash device.

3. Results and Discussion

Fig. 1 shows the cross-section TEM images of (a)

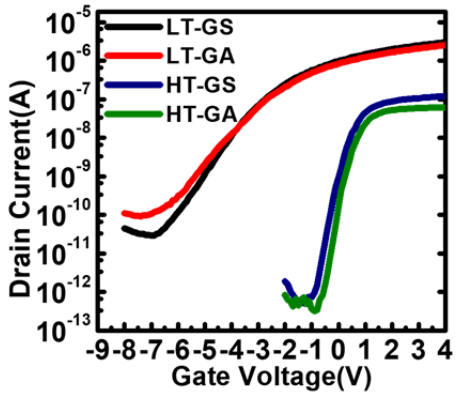

Fig. 3. Initial Id-Vg characteristics of all poly-Si CT devices.

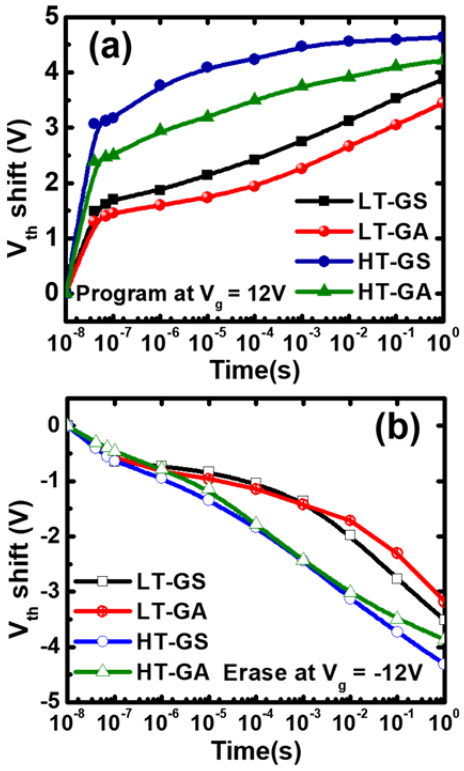

Fig. 4. (a) Programming and (b) erasing speed of all poly-Si CT devices.

LT-GA and (b) HT-GS poly-Si CT flash devices. The origin width of poly-Si channel is similar. However, the low temperature deposited Ge film is thicker than expected. Hence, the channel width of both LT-GS and LT-GA devices are larger than that of HT ones. The energy dispersive spectroscopy (EDS) analysis of LT-GA device is shown in Fig. 2. The Ge content in LT devices are much more than that in HT ones. Fig. 3 shows transfer characteristics of all poly-Si CT flash devices. The subthreshold swing (S.S.) values of LT devices are much more than those of HT ones. The larger S.S. may be caused by the larger fin width, incomplete oxidation, and residue Ge film on poly-Si channel. Fig. 4 shows (a) programming and (b) erasing speeds of all devices. Both HT devices show faster programming speeds. A larger fin width would form a smaller curvature of poly-Si channel, and then results in less electric field enhancement on LT-GS and LT-GA devices. Therefore, both LT-GS and LT-GA

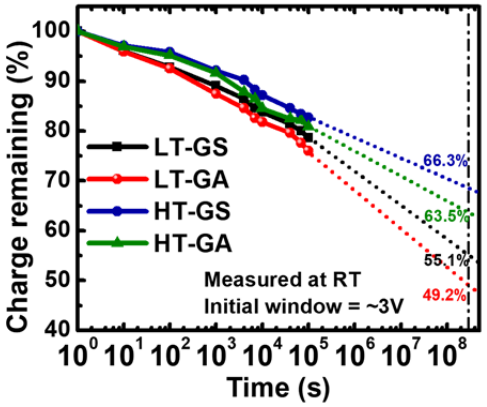

Fig. 5. Retention characteristics of all poly-Si CT devices.

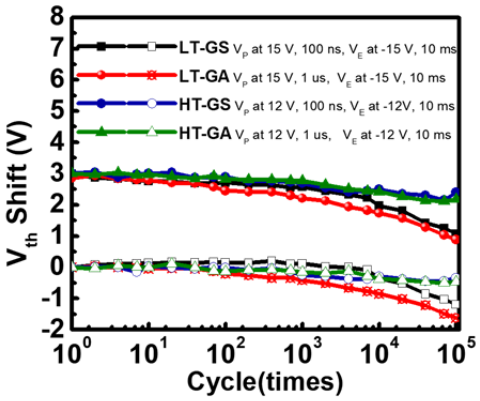

Fig. 6. Endurance characteristics of all poly-Si CT devices.

show slower P/E speeds even with lower energy barrier across the tunneling layer. Fig. 5 shows retention characteristic of all devices. All devices were with initial window of 3 V. Since a lower electron barrier is caused by more Ge content in tunneling oxide, the retention performance of LT-GS and LT-GA devices is degraded. The endurance characteristics of all devices with initial window of 3 V are shown in Fig. 6. All devices remain enough memory windows even after 10^4 P/E cycle. However, both LT-GS and LT-GA devices show larger window shift after 100 P/E cycles. The window shift may be caused by larger operation voltage and then more defect and trap generation.

3. Conclusions

Poly-Si CT flash devices with Ge surface channel formed by different temperatures were studied. Although P/E speeds can be enhanced by a higher Ge content in the tunneling layer, the thickness of ICP deposited Ge should be carefully controlled. Since the fabrication process with low thermal budget is desirable for high density CT flash devices, optimal recipes for low temperature deposition are required.

References

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