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A Simple Methodology of On-Chip Transmission Line Modeling for High Speed Clock Distribution

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Abstract

High-speed clock distribution design is becoming increasingly difficult and challenging task due to the necessity of on-chip transmission line design and time-consuming Electro-Magnetic (EM) simulation. In this paper, we present a simple, accurate on-chip transmission line modeling without using EM-simulation. A 5-wire of GSGSG interconnect structure is converted to *RLC*-distributed equivalent single-ended model for simplification and easy calculation. We applied our proposed model to 9 mm on-chip clock distribution line at 3GHz in TSMC 0.18µm 1-Poly 6-Metal CMOS process and the proposed model showed good match with EM-model.

1. Introduction

In a modern digital system, clock distribution is one of the most important functions in the chip. For instance, a high-speed I/O clock distribution structure shown in Fig.1 is used for Transceiver blocks. [1] In this clock distribution design methodology, conventional design places repeaters at a certain distance so we can use lumped-*RC* model. In recent applications, as the chip area and operating speed get bigger and faster, on-chip transmission line must be treated as *RLC*-distributed model. However, there are several problems for *RLC* extraction. First, it requires time-consuming EM-simulation. Second, on-chip transmission line design needs a huge number of parameter optimization such as metal width, space, thickness, length, layers and shielding structures. Third, adopting extracted S-parameter to time domain is sometimes difficult task due to convergence problem during convolution process. Therefore, a simplified, accurate equivalent *RLC*-distributed model is desirable for circuit designer to expect the best interconnect structure without using EM-simulation. In this paper, we introduce a simple, accurate on-chip transmission line modeling where a 5-wire of GSGSG physical interconnect structure is converted to *RLC*-distributed equivalent single-ended model.

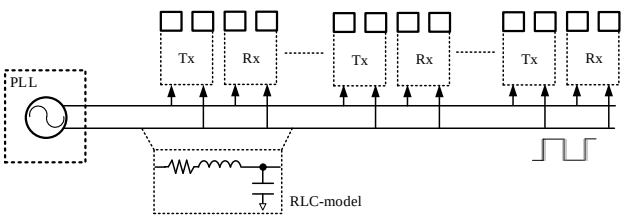


Fig.1 High speed I/O clock distribution structure

2. Transmission line modeling

Fig.2 shows the conversion methodology from a 5-wire of GSGSG interconnect to equivalent *RLC*-single-ended model. First, a 5-wire physical model shown in Fig.2(a) is converted to a 5-wire equivalent circuit model shown in Fig.2(b). Second, Fig.2(b) is converted to calculation model shown in Fig.2(c). From Fig.2(c), we get (1)-(3). By adding line capacitances, we get equivalent *RLC*-differential model shown in Fig.2(d). Here, each *RLC* value is calculated by existing empirical equations (4)-(9) introduced in [2]-[3]. The high frequency physical effects called skin, proximity effect and dielectric-loss are ignored in this modeling. Note that Fig.2(d) is equivalent to Fig.2(e) since it is symmetrical. Thus, the total number of elements is reduced to only 3.

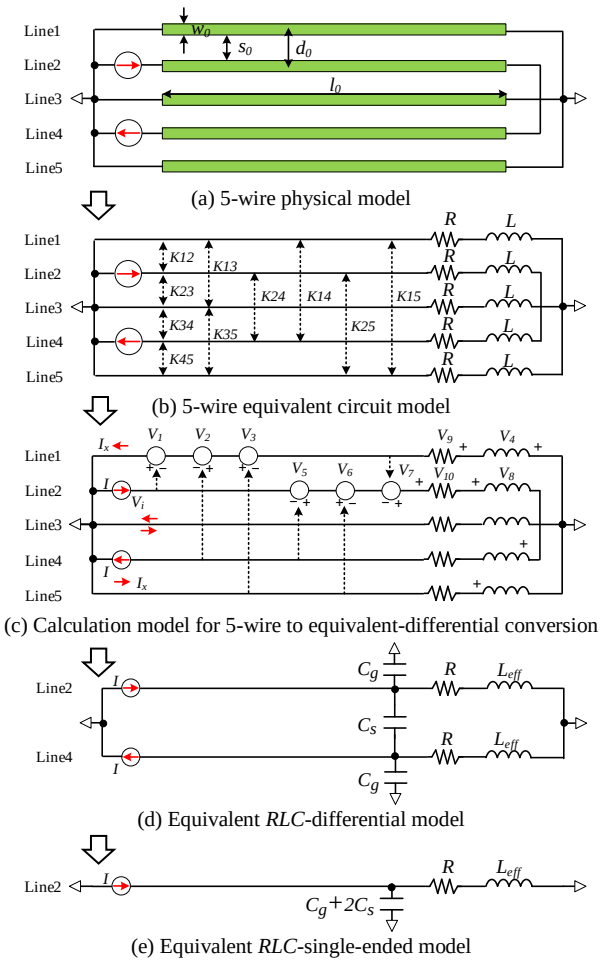


Fig.2 Conversion methodology from 5-wire to equivalent 1-wire

$$I_x = \frac{sL(K_{12} - K_{14})}{R + sL(1 - K_{15})} \cdot I \quad (1)$$

$$V_i = sLI_x(K_{25} - K_{12}) + I\{R + sL(1 - K_{24})\} \quad (2)$$

$$L_{eff} = imag\left(\frac{V_i}{I}\right)/(2\pi f) \quad (3)$$

$$R = R_{sh}\frac{l_0}{w_0} \quad (4)$$

$$C_g = \varepsilon\left\{\frac{w_0}{h_0} + 2.977\left(\frac{t_0}{h_0}\right)^{0.232}\right\} \quad (5)$$

$$C_s = \frac{1}{2}\varepsilon\left\{0.229\left(\frac{w_0}{s_0}\right) + 1.227\left(\frac{t_0}{s_0}\right)^{1.384}\right\}\left(\frac{h_0}{s_0}\right)^{0.0398} \quad (6)$$

$$L = \frac{\mu_0 l_0}{2\pi}\left\{ln\frac{2l_0}{w_0 + t_0} + \frac{1}{2} + \frac{2}{9}\left(\frac{w_0 + t_0}{l_0}\right)\right\} \quad (7)$$

$$M = \frac{\mu_0 l_0}{2\pi}\left\{ln\left(\frac{l_0}{d_0} + \sqrt{1 + \frac{{l_0}^2}{{d_0}^2}}\right) - \sqrt{1 + \frac{{d_0}^2}{{l_0}^2}} + \frac{d_0}{l_0}\right\} \quad (8)$$

$$(d_0 = w_0 + s_0)$$

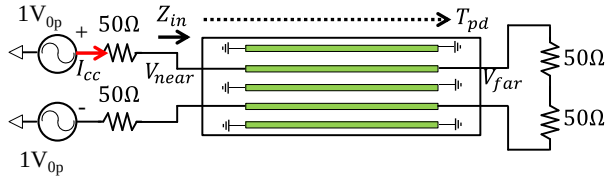
$$K = \frac{M}{L} \quad (9)$$

Here,

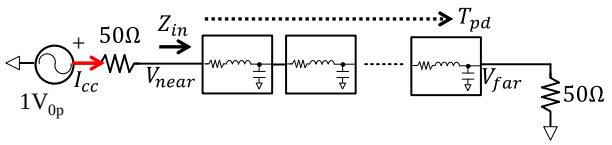
w_0	: width of wire	s_0	: space of wire
h_0	: height of wire	t_0	: thickness of wire
l_0	: length of wire	R_{sh}	: sheet resistance
R	: DC resistance	L	: self-inductance
M	: mutual-L	K	: coeff. of mutual-L
C_g	: capacitance to GND	C_s	: capacitance to side wire
ε	: permittivity	μ_0	: permeability
I_x	: return current	L_{eff}	: effective L
s	: Laplace operator	$imag$	: imaginary part
f	: frequency		

3. Model accuracy

Fig.3 is a test circuits to compare the model accuracy between EM-model and proposed model. We evaluated propagation delay T_{pd}, input impedance Z_{in}, current consumption I_{cc}, near-end and far-end voltage swing V_{near} and V_{far} under Table-1 condition. The comparison results are listed in Table-2. From Table-2 results, the maximum error of proposed model against EM-simulation is only 6%. This is accurate enough for the first design estimation.



(a) EM-model-based (Keysight Momentum-RF)



(b) Proposed-model-based (Fig.2(e) is divided into 30-units.)

Fig.3 Test circuits to compare EM-model and proposed-model

Table-1 (Design parameters)

Parameters	Value
Signal layer	M6
Configuration	GSGSG
Top/Bottom shielding	Top: Air Bot: M1
Width	3 um
Space	3 um
Length	9 mm
Frequency	3 GHz

Table-2 (Comparison results)

Parameter	Unit	EM	Proposed	Error
T_{pd}	[ps]	64.3	68.1	6.0%
Z_{in}	[Ω]	74.0	70.8	-4.4%
I_{cc}	[mA]	8.24	8.43	2.3%
V_{near}	[V_{0p}]	0.61	0.60	-2.2%
V_{far}	[V_{0p}]	0.31	0.32	3.0%

4. Conclusions

In this paper, we presented a new on-chip transmission line modeling without using EM-simulation. The proposed transmission line modeling converts a 5-wire of GSGSG interconnect structure to equivalent *RLC*-distributed single-ended model for simplification and easy calculation. The total number of unit components becomes only 3. The maximum error of our proposed model against EM-model is 6% at length of 9mm, frequency of 3GHz in TSMC 0.18μm 1-poly, 6-metal CMOS process.

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