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# Investigation on Parasitic Loss at the AlN/Si Interface for GaN-HEMTs Application

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**Abstract**

**Parasitic RF Losses of GaN-based HEMTs on Silicon substrates have been investigated in this study. The loss issue caused by the AlN/Si interface can be reduced by optimizing the AlN buffer. Inserting a low-temperature (LT) AlN in the middle of high temperature (HT) AlN buffer reduces the piezoelectric tensile stress caused by the mismatch between AlN and Si, which results in the improvement of RF loss of GaN-on-Si HEMT structure.**

## 1. Introduction

GaN-based HEMTs have outstanding properties for high-power, high-frequency applications and high-temperature operation. These excellent characteristics belonged to GaN are essential to head forward breakthrough of technology. Considered on the fabricated cost, silicon substrates are competitive in the market. Nevertheless, the GaN-HEMTs on Si applied to high-frequency still has the main parasitic issue degrading RF devices performances.[1-3] It is believed that the interfacial p-type conductive channel caused by Ga/Al atoms diffusion is responsible for RF losses.[4] Besides, RF leakage has been analyzed with the inversion layer generated by atomic diffusion at the buffer/Si interface. [5] Actually, AlN buffer played a major role for the nucleation of GaN-HEMT structure. H. Yacoub et al. have proved the inversion channel formation at AlN/Si interface because of observation of bell-shaped CV. [6] In this study, we consider the parasitic loss issue caused by the inversion layer at the AlN/Si interface.

## 2. Experiment

Epitaxial samples were grown on low-resistivity silicon substrate (LRSi) (80ohm-cm) or high-resistivity silicon (HRSi) (1000ohm-cm) by MOCVD. The AlGaN/GaN HEMTs on HRSi were also achieved with graded AlGaN transient layer and C-GaN buffer layer. As shown in Fig.2, RF loss of measurements were executed by CPW lines [real devices shown in Fig. 2(c) (d)] is the simple and immediate means for phenomenon observation. The losses were determined by scattering parameter measurement. Other analysis methods which were utilized to characterize epitaxial film properties including SEM, HR-XRD, Raman Spectrometer, spreading resistance profile (SRP).

## 3. Results and Discussion

*A. Investigation on parasitic loss at AlN/Si*

Figure.1 (a) and Fig.1 (b) and Table I show the material characteristics of structure (200-nm HT AlN on Si) and structure (200-nm HLH AlN on Si.). The use of a LT AlN improved not only crystalline quality but also leakage current. Fig.3 (a) shows leakage current has been suppressed from $10^{-7}$A to $10^{-12}$A. Besides, LT AlN inserted to compensate the tensile stress generated due to piezoelectric HT AlN/Si at interface. Usually, the frequency shift of E2 Raman mode is used to check the residual stress, while the crystalline quality is good enough. The E2 peak position of bulk AlN material should be at 657cm$^{-1}$[8], it means no biaxial stress at the AlN/Si interface. The shift values of E2 Raman mode were 8.7 cm$^{-1}$ and 7.4 cm$^{-1}$, respectively (Table I). The biaxial stress and piezoelectric stress was calculated from the Raman shift and shown in Table II. The total losses, which are caused by the substrate loss, p-type diffusion channel, and the inversion n-type channel, of two structures are shown in Fig.3 (c). Since the spreading resistance profiles of the two structures are similar (Fig. 3b), the losses caused by the p-type channel and the Si substrate have the same contributions for the two samples. Therefore, the reduction of total loss in Fig1. (b) results in the reduction of residual tensile stress and the consequently low leakage current. It implies the impact of the inversion channel which induces an n-type conductive channel at AlN/Si interface has been alleviated by the use of LT AlN. Moreover, the lower piezoelectric tensile stress, the lower sheet carrier concentration were induced due to lower piezo-polarization. Besides, comparing the 3 AlN/Si samples shown in Fig.3 (c), the loss of HT AlN was improved by using high-resistivity Si substrate,

*B. The temperature-dependent parasitic loss of GaN-on-Si*

Figure.4 (a) shows the temperature-dependent losses of AlN/Si samples[Fig.1 (a)~(c)], while the loss of AlN on HR Si strongly increases with the increasing temperature, the losses of both samples HT AlN on p-type Si and HLH AlN on p-type Si remain and become smaller than the loss of AlN on HRSi at all temperatures. Therefore, substrate choice become important for high-frequency applications working at high temperature; on the other hand, loss can be improved even up to the same loss of sample(c) by HLH AlN at 125°C. Fig.4 (b) shows the change of piezoelectric tensile stress with temperature. Sample (b) has less tensile stress than others obviously. LT AlN has the effect on the reduction of the piezoelectric stress. Further, loss issue also was improved by the HLH AlN buffer.

Lastly, the RF losses of full stack GaN-based HEMTs on Si structure are shown in Fig. 6. Obviously, HT AlN buffer without intermediate AlN layer which shown in the blue symbol is largest, while the GaN-HEMTs with HLH AlN

have less loss. Moreover, the sample with 100nm HLH AlN layer compared to 200nm sample, the loss was also improved. It implies optimization of the AlN buffer is the critical issue to improve the parasitic loss.

## 4. Conclusions

The parasitic loss at AlN/Si interface related to the spontaneous piezoelectric stress has been studied. The use of LT AlN intermediate layer inserted the middle of HT AlN buffer plays an essential role to reduce the piezoelectric field, and consequently reduce the inversion channel, leading to the improvement of the RF loss of GaN-on-Si.

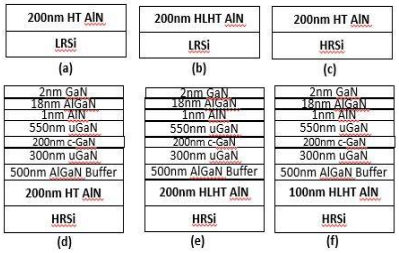


Fig.1 Epitaxial samples in this study (a) 200nm HTAlN/LRSi (b) 200nm HLH-AlN/LRSi (c) 200nm HTAlN/HRSi (d) GaN-HEMT with 200nm HTAlN (e) GaN-HEMT with 200nm HLH-AlN (f) GaN-HEMT with 100nm HLH-AlN

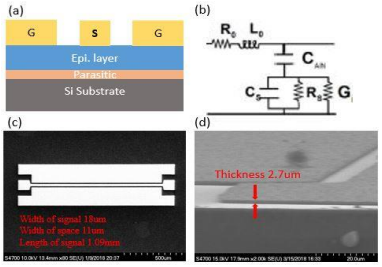


Fig.2 Structure of CPW with (a) schematic cross-section structure (b), equivalent circuit (c), and top-view (d), cross-section of SEM image

Table I. Material Characteristic of AlN

| Symbol | Thickness | XRC(002) | Raman $E_2$ |
|---|---|---|---|
| (a) | 200nm | 1500 arcsec | 648.3 $cm^{-1}$ |
| (b) | 200nm | 900 arcsec | 649.6 $cm^{-1}$ |

Table II. Correlation between piezoelectric stress and losses at room temperature

| Sample | Piezoelectric Stress($10^{-3}$GPa) | Loss at 30GHz(dB/mm) | Loss at 12GHz(dB/mm) |
|---|---|---|---|
| (a) | -5.8 | -1.47 | -1.25 |
| (b) | -4.9 | -1.06 | -0.88 |
| (c) | -5.5 | -0.56 | -0.38 |

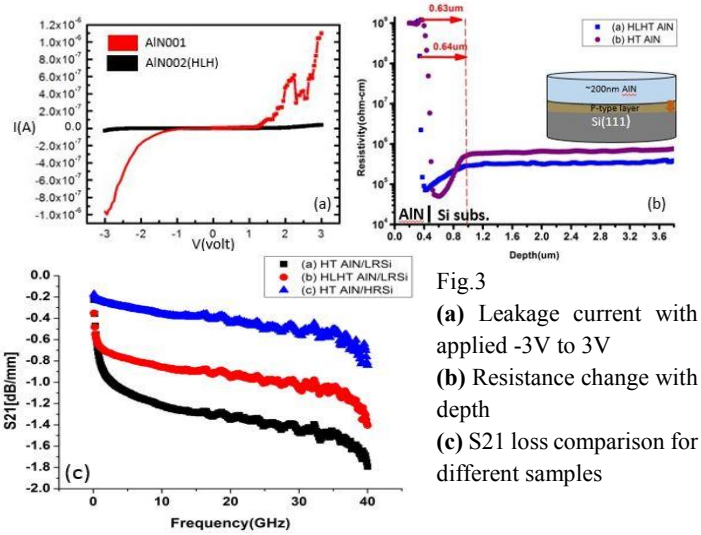


Fig.3
**(a)** Leakage current with applied -3V to 3V
**(b)** Resistance change with depth
**(c)** S21 loss comparison for different samples

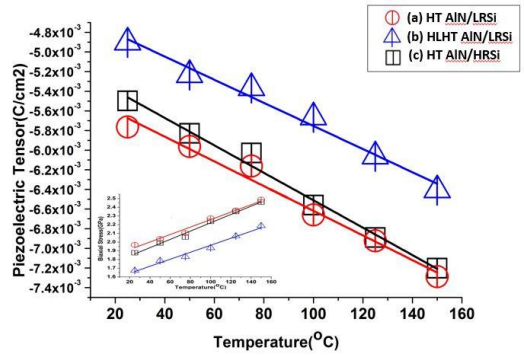


Fig.4 RF loss for different samples with temperature in this study

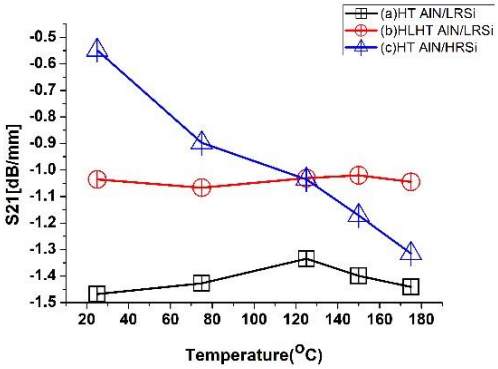


Fig.5 Change of piezoelectric tensile stress with temperature

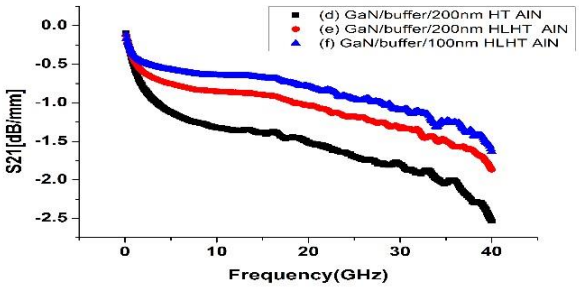


Fig.6 S21 comparison of GaN-HEMTs with different AlN buffers


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