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Fabrication of $In_{0.53}Ga_{0.47}As$ homo-junction TFET with optimized gate stack by employing surface treatment and post metallization annealing

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Abstract

This work demonstrates the experimental I-V characteristics of vertical $In_{0.53}Ga_{0.47}As$ homo-junction tunnel field-effect transistor (TFET) which has high on/off ratio and low subthreshold slope (SS). Both leakage current and SS were enhanced by gate stack interface optimization. Sulfur treatment and TMA precursor pulsing suppressed interfacial oxide at $In_{0.53}Ga_{0.47}As$-dielectric interface and post-metal-annealing (PMA) process cured damage from e-beam evaporation metallization.

1. Introduction

Since Internet of Things (IoT) technology is drawing attention in semiconductor industries, demand on low-power and high-performance switching device is increasing rapidly. Conventional method to boost performance of Si CMOS devices is downscaling. However, downscaling approaches are facing physical limits of short-channel devices. Recently, many researches focus on alternative approaches for reducing power consumption and improving device performance such as TFET, and negative capacitance field-effect transistor (NCFET) [1-2].

TFET device can be a breakthrough for reducing SS lower than 60 mV/decade by band-to-band tunneling (BTBT) current mechanism. However, tunneling barrier severely limits on-current of TFET. Employing III-V material may result in higher tunneling current compared to Si because of lower bandgap and smaller effective electron mass [3]. Still, lack of high-quality interfacial insulator with low interfacial trap density makes it difficult to move on to III-V channel devices. Any traps in TFET device can lead to high leakage current and SS by trap-assisted tunneling (TAT) current. Therefore, improving gate stack quality is the most challenging part of III-V TFET study.

In this work, we represent high-quality gate stack by employing sulfur treatment, and in-situ TMA pulsing treatment at high-k/InGaAs interface. Both treatments are known to reduce native oxide of InGaAs surface and improves high-k/InGaAs interface quality [4-5]. Also, PMA process was conducted to cure damage of both high-k/InGaAs interface and high-k/metal interface. As a result, we have demonstrated $In_{0.53}Ga_{0.47}As$ homo-junction TFET devices with high on/off ratio and low SS.

2. Experiment

We fabricated $In_{0.53}Ga_{0.47}As$/MOS capacitors with SiN_x/HfO_2 dual-layer dielectric and conducted annealing process at different fabrication steps (prior to metal deposition and after metal deposition) to determine the effects of annealing to the gate stack. PMA effects of different gate metals are also investigated. The epitaxial structure of MOS capacitance was Si-doped n-type $In_{0.53}Ga_{0.47}As$ channel layer with 1.0E+17/cm^3 doping concentration grown on InP substrate. High-quality PEALD SiN_x interfacial layer was deposited in ICP-CVD chamber after surface cleaning with diluted HCl, and NH_4OH (29%) solutions. Bulk HfO_2 layer was deposited in ALD chamber using $Hf[N(C_2H_5)(CH_3)]_4$ (TEMAH), and O_3 as precursors subsequently with deposition rate 0.9Å/cycle. Annealing in RTA chamber with foaming gas ambient (N_2 95%, H_2 5%, 5mTorr) at 400ºC for 10min was carried out for PDA process. Both gate metal (Pt/Au, Ni/Au, sputtered TiN) and bottom contact metal (Ti/Au) were deposited in e-beam evaporation system. Finally, PMA process with same condition of PDA was performed. Fig. 2 shows the results for MOS capacitors.

After further optimization of high-k dielectric by changing precursor from O_3 to Isopropyl Alcohol (IPA) and employing nitrogen plasma, $In_{0.53}Ga_{0.47}As$ homo-junction TFET with optimized HfO_xN_y/Pt/Au gate stack was fabricated as shown in Fig. 1. The device was fabricated on molecular beam epitaxy (MBE)-grown n^+-i-p^+ epitaxial layer with in-situ highly abrupt junctions. The epitaxial layer consists of 15nm n^+ (Si doping of 5E+19/cm^3) $In_{0.7}Ga_{0.3}As$ drain contact layer, 30nm n^+ (Si doping of 5E+19/cm^3) $In_{0.53}Ga_{0.47}As$ drain layer, 50nm intrinsic layer, 300nm p^+ (Be doping of 1E+19/cm^3) $In_{0.53}Ga_{0.47}As$ source, and 300nm intrinsic $In_{0.52}Al_{0.48}As$ grown on semi-insulating InP substrate. First, MESA sidewall was etched by citric acid/H_2O_2 water solution with total etching depth of ~145nm. 3 cycles of digital etching, which consists of O_2 plasma treatment for oxidation step and oxide-etching step with diluted HCl, were performed with pre-gate treatment using NH_4OH solution, $(NH_4)_2S$ solution, and in-situ TMA pulsing prior to gate dielectric deposition. Optimized 6nm HfO_xN_y dielectric was deposited in ALD chamber using TEMAH, and IPA as precursors with deposition rate 1.0Å/cycle. Gate metal (Pt/Au) was deposited in e-

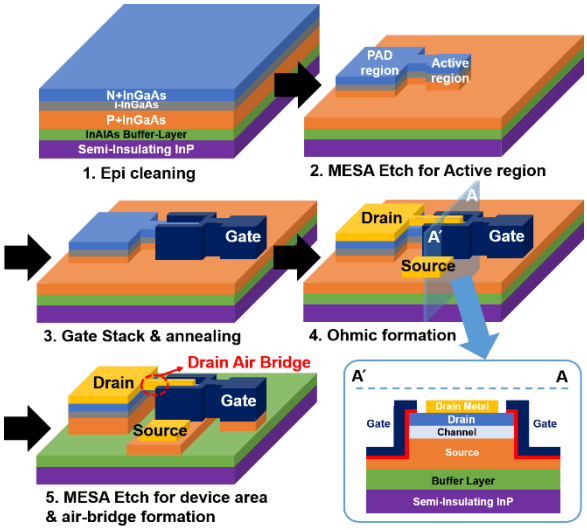

Fig. 1 Process flow and cross-sectional view of $In_{0.53}Ga_{0.47}As$ homo-junction TFET.

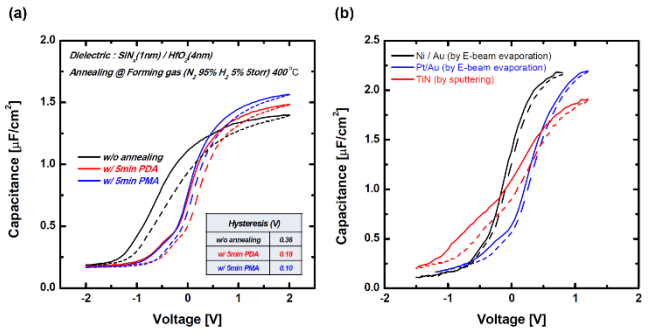

Fig. 2 C-V_G characteristics for (a) different annealing conditions, and (b) different gate metals

beam evaporation system, followed by PMA at 400ºC for 10min in forming gas ambient. After gate stack formation, ohmic contact was formed by e-beam evaporated Pd/Au. Finally, drain air-bridge was formed by using phosphoric acid/H_2O_2 water solution to make undercut of $In_{0.53}Ga_{0.47}As$, which isolates device from contact pad to reduce leakage current. The results are shown in Fig. 3.

3. Results and Discussions

Damage curing effects of annealing at different conditions were investigated by C-V_G characteristics of HfO_2/InGaAs MOS capacitor. While hysteresis was 0.36V without any annealing, it was reduced to 0.18V after PDA process, which represents effective damage curing of annealing process. Remarkably, PMA process suppressed hysteresis further. This additional suppression of hysteresis is attributed to curing of high-k/metal interface damage produced during e-gun evaporation process. Annealing effects of different metals were also investigated. Sputtered TiN gate metal showed serious degradation in C-V_G characteristic. Surface defects are generated significantly during high power sputtering process. Also, flat band shift due to different metal workfunction

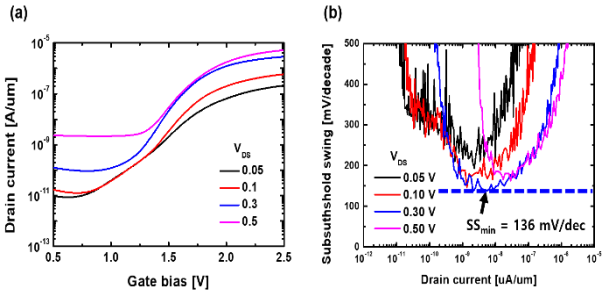

Fig. 3 (a) I_D-V_G characteristics, and (b) Extracted SS of fabricated $In_{0.53}Ga_{0.47}As$ homo-junction TFET

was observed.

I_D-V_G characteristics and extracted SS of fabricated HfO_xN_y $In_{0.53}Ga_{0.47}As$ homo-junction TFET are shown in Fig. 3. It showed high SS (136mV/dec), high I_{on} (2.88E-6A/um), and high on/off ratio (3.11E+4) at V_{DS} = 0.3V, which is remarkable performance of photo-aligned large size device. These results were achieved by optimized gate stack process.

4. Conclusions

In summary, high performance vertical $In_{0.53}Ga_{0.47}As$ homo-junction TFET was fabricated by optimizing gate stack. Surface treatments with $(NH_4)_2S$, and in-situ TMA pulsing were performed to optimize high-k/InGaAs surface. Also, PMA cured damage in gate stack. We expect that gate optimization could replace Si CMOS devices to III-V TFET devices.

Acknowledgements

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