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High-bias-stability Al_2O_3 films formed by high-temperature annealing after atomic layer deposition

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Abstract

We intensively investigated a high-temperature annealing effect on the bias instability of atomic-layer-deposited (ALD) Al_2O_3 films, which, as an alternative to the well-established thermal SiO_2 on Si, are a promising candidate for gate insulators of wide-bandgap semiconductor (WBGS) devices. The flat-band voltage shift of stressed Al_2O_3 metal-insulator-semiconductor (MIS) capacitors is approximately a Kohlrausch-type complementary extended exponential function of stress time, thereby enabling to estimate the maximum flat-band voltage shift based on a finite-time data set. The maximum flat-band voltage shift thus obtained for the samples annealed at 750°C after ALD is found to be smaller than 0.2 eV even at 200°C under an expected rating voltage, i.e., an equivalent SiO_2 field of 4 MV/cm, exhibiting excellent bias stability. Hence, the technology developed here will enhance the performance and reliability of WBGS MIS field-effect transistors.

1. Introduction

Wide-bandgap semiconductors, such as GaN and diamond, have recently been attracting attention from power device engineers as a substitute for the traditional Si. Since the well-established thermal SiO_2 is difficult to form as a gate insulator on these materials, various insulators have been investigated using atomic layer deposition (ALD), which forms films with unparalleled uniformity and reproducibility. Among those films, ALD-Al_2O_3 is an attractive candidate, having a wide bandgap of 7eV [1], a high dielectric constant of 9 [2], etc. A major challenge for the Al_2O_3 in practical applications is the suppression of threshold voltage shift of Al_2O_3–insulated metal-insulator-semiconductor field-effect transistors (MISFETs) during long-term operation. The purpose of this study is to achieve this by performing high-temperature annealing after ALD.

2. Experimental methods

For ease of experiments, instead of the threshold voltage of MISFETs, this study investigates the flat-band voltage of Al / 29-32-nm-thick Al_2O_3 / 1.2-nm-thick SiO_2 / n-Si MIS capacitors fabricated as follows. After cleaning (001) n-type 2–4 Ωcm Si substrates in an NH_4OH/H_2O_2 mixture, which formed a SiO_2 film, an Al_2O_3 film was deposited by ALD at 450°C with trimethylaluminum and H_2O as precursors. The samples were subsequently annealed for 30 minutes at 600–1000°C in a 4% H_2/Ar atmosphere. Finally, gate electrodes were formed by thermally evaporating Al through a shadow mask with openings.

The thicknesses of the SiO_2 and Al_2O_3 films were measured immediately after their formation, using a spectroscopic ellipsometer. The flat-band voltage shift was estimated by alternately repeating capacitance–voltage (C–V) measurement and constant-voltage stressing of the MIS capacitors. The results from different samples in this study were compared for the same equivalent SiO_2 field (EOF), F_{eo}, defined by $F_{eo} = V_{ins}/EOT$, where EOT is the equivalent SiO_2 thickness of the Al_2O_3/SiO_2 stack and V_{ins} is the voltage applied to the stack, being given by $V_{ins} = V_G - (W_G - \chi_S)/q$ with V_G as the gate voltage, W_G as the gate work function, χ_S as the substrate electron affinity, and q as the electronic charge. EOT was estimated by fitting theoretical C–V curves [3] to experimental ones. Under the same EOF, the results from different samples can be compared for the same MISFET performance [4].

3. Results and Discussion

The flat-band voltage shift, ΔV_{fb}, of the Al_2O_3-MIS capacitors for F_{eo} = 4 MV/cm, a Si device guideline, is shown in Fig. 1 (symbols) as a function of stress time. It is remarkably reduced by the post-deposition annealing (PDA) at 750°C or lower. To estimate the value after 10–20 years, a reliability target, the flat-band voltage shift, ΔV_{fb}, is approximated by a Kohlrausch-type [5] complementary extended exponential function, given by

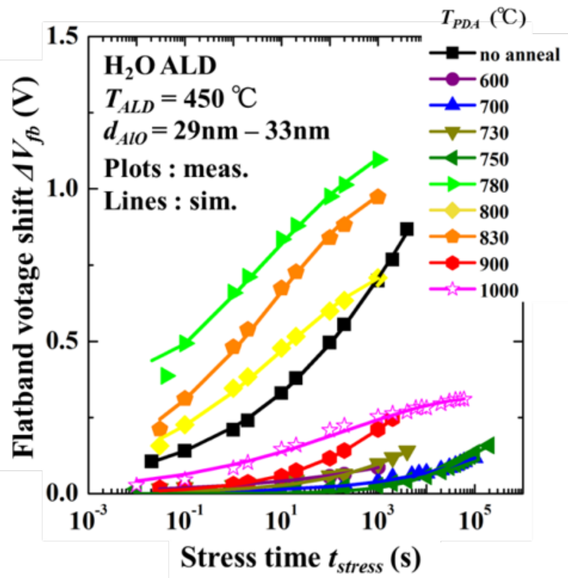

Fig. 1. Flat-band voltage shifts of Al_2O_3 MIS capacitors under F_{eo} = 4 MV/cm vs. stress time. The symbols and lines represent experimental and simulated results, respectively. (The open plots represent negative values.)

$$\Delta V_{fb} = \Delta V_{fb,max}\left\{1 - \exp\left[-\left(\gamma_0 t_{stress}\right)^{\beta}\right]\right\}, \quad (1)$$

where $\Delta V_{fb,max}$ is the maximum of ΔV_{fb}, γ_0 is the effective value of trap creation/charge capture rate γ, t_{stress} is the stress time, and β is a constant that determines the spread of γ distribution. The optimized simulations using Eq. (1) (lines in Fig. 1) excellently fit the experimental results (symbols), validating the approximation using Eq. (1). As shown in Fig. 2, the maximum flat-band voltage shift thus obtained is reduced by PDA at temperatures up to 750°C, but abruptly increases by PDA at 780°C or higher.

This sudden increase is possibly caused by Al_2O_3 crystallization, as revealed by the γ-phase crystalline Al_2O_3 peaks observed in grazing incidence X-ray diffraction patterns of the samples for PDA at 800°C or higher (Fig. 3). Due to the inevitable power consumption by devices themselves, package heat resistance, and a high temperature environment required of power devices, the device temperature mostly increases to 100°C or higher. To assess the bias instability at these temperatures, Fig. 4 shows the maximum flat-band voltage shift of 750°C-PDA samples, measured at room temperature (RT) to 200°C, as a function of equivalent SiO_2 field.

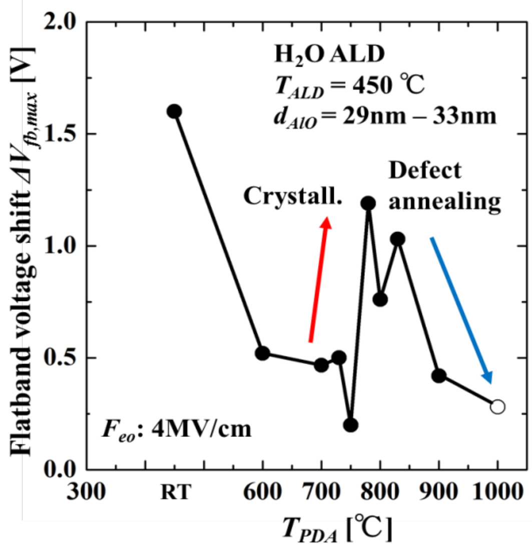

Fig. 2. Maximum flat-band voltage shifts of Al_2O_3 MIS capacitors under F_{eo} = 4 MV/cm vs. PDA temperature. (The open plot represents a negative value.)

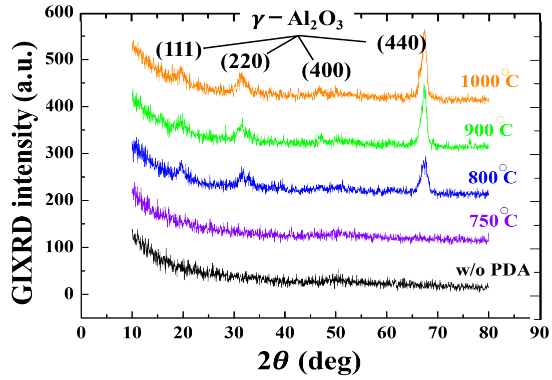

Fig. 3. X-ray diffraction patterns of annealed ALD-Al_2O_3.

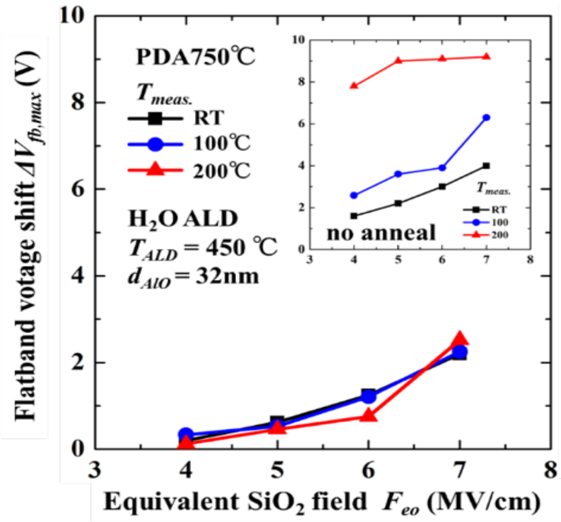

Fig. 4. Maximum flat-band voltage shifts of Al_2O_3 MIS capacitors prepared using 750°C PDA vs. equivalent SiO_2 field. For comparison, the inset shows the results from unannealed samples.

Interestingly and conveniently, the maximum flat-band voltage shift of the PDA samples remains unchanged, smaller than 0.2 V for F_{eo} = 4 MV/cm, even in higher-temperature environments, in stark contrast to the results for non-PDA samples (inset of Fig. 4), which exhibited a remarkable increase in the maximum flat-band voltage shift above 100°C. In this manner, we confirmed a high bias-stability of Al_2O_3 films annealed at 750°C or lower after ALD.

4. Conclusion

The flat-band voltage shift of stressed Al_2O_3 MIS capacitors is approximated by a Kohlrausch-type complementary extended exponential function of stress time, thereby enabling to estimate the maximum flat-band voltage shift based on a finite-time data set. The maximum flat-band voltage shift thus obtained for the samples annealed at 750°C is smaller than 0.2 eV even at 200°C under an equivalent SiO_2 field of 4 MV/cm, exhibiting an excellent bias stability. Hence, the technology developed here will enhance the performance and reliability of wide-bandgap semiconductor MISFETs.

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