Characteristic Analysis of Normally-off Al₂O₃/H-diamond MOSFET with 40-µm Gate Length

Jinfeng Zhang¹, Wanjiao Chen², Zeyang Ren³, Jincheng Zhang⁴ and Yue Hao⁵

¹ Xidian Univ. No.2 Southern Tai Bai Rd Xi'an, Shanxi, China

Phone: 188-2902-1589 E-mail: jfzhang@xidian.edu.cn

Abstract

A normally-off Al₂O₃/H-diamond metal-oxide-semiconductor field effect transistor (MOSFET) with a gate length of 40 μm was characterized. The device metrics include a threshold voltage of -1.42 V, a maximum drain current of -2.2mA/mm, a peak transconductance of 1.78 mS/mm and a maximum capacitance of 3.9 $\mu F/cm^2$. On the basis of C-V characteristics, a quirt high density of the positive fixed charge present in the Al₂O₃ layer (5.48×10¹²cm⁻²) and interface traps of 9×10¹¹ cm⁻² at Al₂O₃/H-diamond interface have been calculated. An empirical formulation expressed the dependence of effective mobility on the gate voltage are proposed.

1. Introduction

Hydrogen-terminated diamond (H-diamond) field effect transistor (FET) with holes accumulate spontaneously on the diamond surface is the mainstream structure for diamond devices. To date, a 200 nm-gate diamond FET with a maximum drain current (I_{DS}) of -1 A/mm and an RF output power density of 2 W/mm [1] has been reported and more normally-on devices continue to be explored and optimized.

The normally-on diamond devices have already achieved a great process. In comparison, normally-off devices need more attention to realize the advantages of higher security and lower power. Yuya Kitabayashi et al. exhibited normally-off operation of a partial C-O channel C-H diamond MOSFETs with ALD-Al₂O₃ as gate dielectric. [2] J. W. Liu et al. realized normally-off LaAlO₃/Al₂O₃/H-diamond MOSFET by annealing the sample at 180 °C for 10 min. [3] Inspired by all these facts, we fabricated a partial C-O channel Al₂O₃/H-diamond MOSFET with 3 nm Al₂O₃ dielectric layer formed by thermal oxidation of Al at 100 °C. In this letter, we repot the current-voltage (I-V) and capacitance-voltage (C-V) characteristics of the 40-um device. The fixed charge and interface traps in MOSFET are analyzed and the μ_{eff} affected by drain and gate voltage are exhibited.

2. General Instructions

Experiment

The material used for our study is (001)-oriented single-crystal of irregular polygon, which grown by a microwave plasma-enhanced chemical vapor deposition (MPCVD) method on the Ib-type substrate ourselves. The surface of the sample was exposed to the hydrogen plasma at 890 $^{\circ}$ C for 20 min to obtain hydrogen terminated diamond. A 100-nm-

thick gold layer was deposited by electron beam evaporation (e-beam) on the H-diamond surface to protect the surface during the following process and to provide source and drain ohmic contacts. Then we realized isolation process by exposing a portion of diamond surface to oxygen plasma after photolithography and wet etching used KI solution. The source and drain electrodes was obtained simultaneously when gate window was etched, and a partial C-O channel was formed at gate window by 3-min UV ozone treatment. E-beam technique was used to deposit 3nm Al on sample followed by oxidation in air at 100 °C for 8 min to form Al₂O₃ dielectric layer. Finally, a 100-nm-think aluminum were sequentially deposited by e-beam and lifted off to achieve gates of the devices. The gate length (L $_{\!G})$ and width (W $_{\!G})$ are 40 and 50 $\mu m,$ respectively. The schematic cross-section view of the device structure is shown as the inset of Fig.1.

DC operation

The output characteristics for the Al_2O_3/H -diamond device with large gate length of $40\mu m$ are shown in Fig.1. A I_{Dmax} of -2.2 mA/mm are obtained at V_{GS} = -3.5 V. The drain current (I_{DS}) as well as the corresponding transconductance (G_m) versus V_{GS} are shown in Fig.2. A threshold voltage of -1.42 V and a maximum G_m of 1.78 mS/mm are achieved.

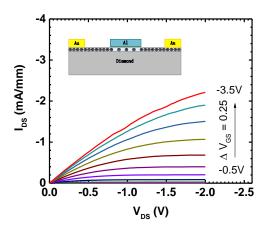


Fig.1 output characteristics and (inset) device structure of the 40-um normally-off H-diamond FET with Al₂O₃ gate dielectric.

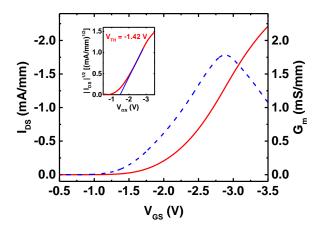


Fig.2 Transfer characteristics of the H-diamond FET.

C-V Characteristics

Figure 3 shows C-V characteristics measured at the frequency of 1MHz for the Al₂O₃/H-diamond MOS structure with gate voltage scanning from positive to negative and then back to positive. The maximum capacitance of 0.39 $\mu F/cm2$ is comparable to the value (0.361 $\mu F/cm2$) of the large gate length MoO₃/H-diamond MOSFET. [4] The fixed charge value is 5.48×10¹² cm⁻² calculated by Cox (V_{FB2}-V_{FB0})/e. The summed density of interface traps is 1.12×10^{12} cm⁻² calculated by Cox (V_{FB2}-V_{FB1})/e.

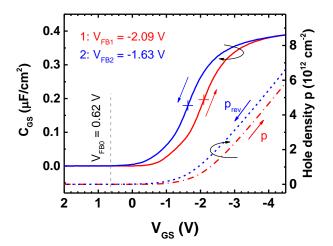


Fig.3 C-V characteristics of the normally-off device, and the hole density corresponding to the capacitance.

Mobility analysis

Besides the scattering mechanisms in bulk semiconductors such as lattice and impurity scattering, the hole in the channel is additionally scattered by collisions with the walls of the channel, which reduces the low-field mobility. And the low-filed mobility for holes can be fitted as $\mu \approx 2485 F_{eff}^{-0.23}$. A similar relationship for Si p-channel MOSFET is independent of substrate doping, substrate bias, and oxide thickness.

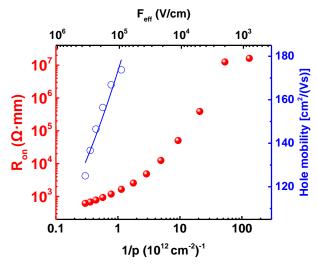


Fig.4 On-resistance as a function of the reciprocal of hole density and the hole mobility as a function of the effective vertical field. The effective vertical field is corresponding to the reciprocal of hole density.

3. Conclusions

In conclusion, the 40-µm normally-off H-diamond MOSFET with Al_2O_3 gate dielectric formed by thermal oxidation of Al has been fabricated. A UV ozone treatment purposing to accomplish the enhanced FET implemented before gate dielectric layer deposited. The $I_{\rm Dsat},\,V_{\rm TH},\,g_{\rm m}$ and $C_{\rm GS}$ for the 40-µm FET were determined to be -2.2 mA/mm, -1.42 V, 1.78 mS/mm and 3.9 µF/cm², respectively. The C-V characteristics reflect the existence of the fixed charge (5.48×10¹²cm⁻²) and the interface traps (9×10¹¹ cm⁻²). The effect vertical field dependence of the $\mu_{\rm eff}$ was fitted inspired from the experience of the analysis of Silicon based MOSFETs.

References

- [1] Hirama, Kazuyuki, et al. IEEE Electron Device Lett. 33(2012)1111.
- [2] Kitabayashi, Yuya, et al. IEEE Electron Device Lett. 38(2017)363.
- [3] Liu, J. W., et al. J. of Appl. Phys. 114 (2015)1759.
- [4] Zhang, Jin Feng, et al. Jpn. J. Appl. Phys. 56 (2017) 100301.