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Nonalloyed Ohmic Contacts to Buried n-GaAs Appearing After Reversed Wafer Transfer Process

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Abstract

For the metamaterial application to the semiconductor devices, formation of nonalloyed ohmic contacts to the both top- and bottom-side of the devices are highly desired. In this paper, we show how to realize nonalloyed ohmic contact to the buried n-GaAs appearing after reversed wafer transfer process. The conditions for the nonalloyed ohmic contacts to the bottom-side is different from those for the top-side reported previously. The key issues are optimizing the Si doping and minimizing the temperature-induced changes. By using this achievement, n-GaAs-based metamaterial optoelectronic devices can be realized with rather easy processes.

1. Introduction

In the n-GaAs based monopolar photonic devices, such as quantum cascade lasers (QCDs) and quantum well infrared photodetectors (QWIPs), formation of metal ohmic contacts to the both top- and bottom n-GaAs layers is inevitably important technologies [1]. The ohmic contacts to the n-type GaAs are normally obtained by alloyed ohmic methods, such as deposition of AuGe/Ni (Pd)/Au followed by sintering at around 400°C [2, 3] since maximum donor density in the Si-doped GaAs is limited to $5\sim10\times10^{18}/cm^3$ [4]. However, the formation of sintering-induced alloyed layers is not desirable when we consider the metamaterial application [5-7]. In the metamaterial application, well-defined metal-semiconductor-metal structures with abrupt interfaces modify and/or enhance the device characteristics. In order to realize abrupt interfaces without the alloyed layers for these purposes, the ohmic contacts should be obtained by nonalloyed methods. In the previous studies, nonalloyed ohmic contacts to top surface after the crystal growth (we call 'top-side')) have been reported.

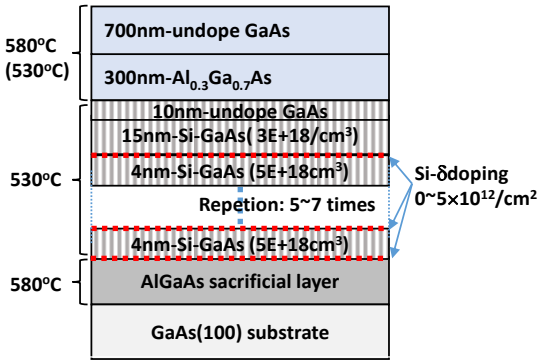

Fig. 1 Schematic illustration of the sample structure.

By using (1) *in-situ* metallization [8], (2) δ-doping of ultra-high density Si [9], or (3) low-temperature grown GaAs (LT-GaAs) layers [10], low contact resistivity are realized. However, the ohmic contacts to another side of n-GaAs have not been established yet. These surfaces are buried after the crystal growth (we call 'bottom-side'). They appear after reversed wafer transfer process. In the recent reports, the bottom-sides are usually nonalloyed Schottky or alloyed ohmic contacts [5-7].

In this paper, we report how to realize nonalloyed ohmic contacts to the bottom-side n-GaAs layers. During the crystal growth, we need to grow device-core structures with high crystal-quality on the layers. Therefore, the n-GaAs layers should not be low crystal quality. For example, LT-GaAs or GaAs doped with ultra-high density Si cannot be used. By optimizing the Si-doping concentration and growth temperature, nonalloyed ohmic contact to the bottom-side were realized.

2. Experimental methods

The samples were grown on semi-insulating GaAs (100) substrates using a solid source molecular beam epitaxy system. The sample structures are schematically shown in Fig. 1. The bottom-side n-GaAs contact layers were grown at 530°C on AlGaAs sacrificial layers, which consist of $5\sim7\times$[4 nm-n-GaAs (Si: $5\times10^{18}/cm^3$) + δ-doped Si ($0\sim5\times10^{12}/cm^3$)] + 15 nm-n-GaAs (Si: $3\times10^{18}/cm^3$) + 10 nm-GaAs (non-doped). After that, 300 nm-$Al_{0.3}Ga_{0.7}As$+700 nm-GaAs (substituted for the device-core structures) were grown at 580°C (or 530 °C). The carrier density in the contact layers were checked by conventional van der Pauw (VDP) methods. For the measurements, InSn were thermally diffused from the top surfaces. For evaluation of contact resistivity, the grown samples were glued to the dummy wafers with upside down, followed by removing the GaAs substrates and AlGaAs sacrificial layers by mechanical and chemical etching. Then, Ti/Au metals are evaporated to the exposed bottom-side n-GaAs (Fig. 2). After

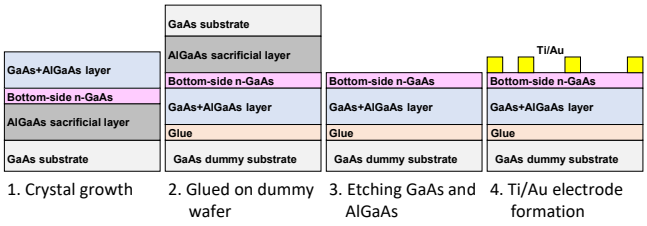

Fig. 2 Schematic illustration of the process after growth.

the metal deposition, the samples were not sintered. The contact resistivity are estimated by using transmission line measurement (TLM) both at RT and 77K.

3. Results and discussion

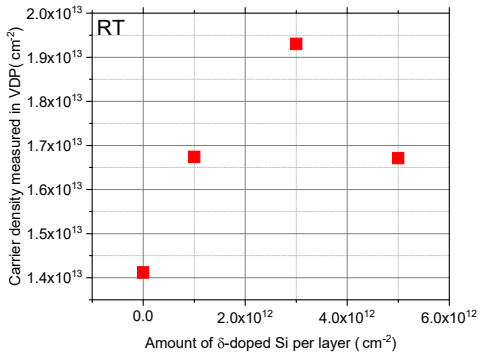

Fig. 3 Carrier density depending on the amount of δ-doped Si.

Fig. 3 shows the carrier density of the samples at RT measured by the VDP method. In this series of the samples, the δ-doping was performed also on the sacrificial layer. The number of δ-doping is six and the thickness of highly doped region is 20 nm. The total density of doped Si ranges from 1.45×10^{13} to 4.45×10^{13}/cm^2. By increasing the Si density per δ-doping layer from 0 to 3×10^{12}/cm^2, the effective carrier density increases from 1.41×10^{13} to 1.93×10^{13}/cm^2. But further increasing the δ-doping results in the decreasing the carrier density down to 1.67×10^{13}/cm^2, indicating that carrier compensation effects become dominant. In principle, the carrier density should be as high as possible for reducing the contact resistivity. Therefore, we performed TLM measurement on the sample with δ-doping density per layer of 3×10^{12}/cm^2 after the reversed wafer transfer process. From here, the repetition number of δ-doping is fixed at seven and δ-doping was not performed on the sacrificial layers. The thickness of highly doped region is 28 nm. As seen in Fig. 4 (a), the I-V curve between the two electrode exhibit nearly ohmic-like behavior at RT. The contact resistivity is 0.2 Ωcm^2. At 77K, however, the resistivity increases and the contact become Schottky. Here, note that we observed much better contact resistivity of 5.6×10^{-4} Ωcm^2 at RT when we applied almost the same structure to the top-side contacts. We attribute the difference between the top- and bottom-side to the annealing-induced changes. While the samples were cooled down immediately after the growth of top-side n-GaAs, the bottom-side n-GaAs is annealed at 580ºC for more than 1 hour for the growth of AlGaAs+GaAs layers. This annealing might be the origin of the changes. In order to suppress the temperature-induced changes, we grew the upper layers also at 530ºC. At 530ºC, we can maintain the quality of GaAs and AlGaAs at reasonably high level. Fig. 4(b) shows the I-V curves between the two electrode at RT and 77K of the sample in which the upper layer was grown at 530ºC. It is clear that ohmic behavior is observed even at 77K. The contact resistivity at RT and 77K is 0.02 and 0.11 Ωcm^2, respectively. Here, it should be noted that there is no significant difference in the carrier densities measured by VDP in these two samples (around 2.3×10^{13}/cm^2). In addition, the actual carrier volume density in the 28 nm-high-doped region is only 6.6×10^{18}/cm^3 assuming that doped Si atoms in the 15 nm-n-GaAs (Si: 3×10^{18}/cm^3) are fully activated. These results suggest that the contact resistivity is not simply governed by the actual carrier density. Possibly the interband states formed by doped Si also have significant effects on the resistivity [11].

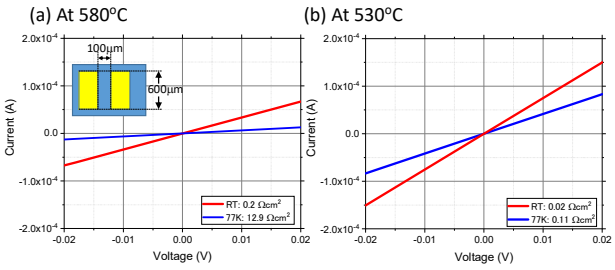

Fig. 4 I-V curves between two electrodes. The upper layers were grown at (a) 580ºC and (b) 530ºC. The inset of (a) shows the measurement configuration.

By using these nonalloyed ohmic contacts, we have fabricated metasurface QWIP (GaAs/AlGaAs) operating at 7.0 μm. The devices exhibit high responsibility of 1.14 A/W (total quantum efficiency: 20.1%) against the normal incident light [12]. The result indicates that high quality GaAs/AlGaAs device-core structure can be grown at 530ºC on the bottom-side n-GaAs.

3. Conclusions

We have realized nonalloyed ohmic contacts to buried n-GaAs appeared after reversed wafer transfer process at RT and 77K. The optimization of Si-doping density and reducing the growth temperature down to 530ºC were the key issues. By using the technique, metasurface QWIP with high detectivity were realized.

Acknowledgements

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