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Hysteretic Single Walled Carbon Nanotube Thin Film Transistor for Ultralow Static Power Consumption Application

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Abstract

Hysteretic behavior in I_d-V_g curves of polycarbazole (PCz) sorted single walled carbon nanotube thin film transistor (SWCNT-TFT) was positively employed for power consumption reduction. Steep subthreshold slope (SS) <10 mV/dec surpassing the Boltzmann limit was observed under slow V_g sweep rate. Detailed studies reveal that surface electrochemical reaction is the main cause of the large hysteresis. An ultralow static power consumption timer application using this SWCNT-TFT is demonstrated, suggesting promising potential for future low power application with hysteretic transistors.

1. Introduction

Hysteretic behavior is widely reported in TFTs that using SWCNT and other semiconductor channels, and negatively considered in most electronic applications except memory because it results in inaccurate transport properties and variability problems [1, 2]. Therefore, various attempts, such as surface passivation, vacuum annealing, have been done to deal with the above problems and significant progress have been made [3, 4]. However, in this study, we positively regard hysteresis as an integrated battery associated with the device. During the discharging cycle of the battery, it is possible to use that for power consumption reduction, especially in the side of static power.

2. Experimental

High purity (> 99%) semiconducting SWCNT solution was separated by using a conjugated polymer, PCz, following the method developed by Zhenan Bao's group [5]. The SWCNTs were dispersed in chloroform. The diameter of the CNTs was about 1.4 nm and the tube length was about 2 μm. Traditional solution deposition method was used to fabricate CNT network films. By soaking the SiO_2/Si substrate in the solution for 24 hours, uniform CNT film with a tube density of ~20 CNTs/um was obtained. Then conventional photolithography was used to open the source/drain windows and followed by a Ti/Pd (0.3/40 nm) layer evaporation and lift-off. After that, the CNT channel was patterned by another photolithography step and oxygen plasma etching. For the back gate devices, thermally grown oxide (thickness of ~300 nm) and the bottom heavily doped Si served as gate dielectric and gate electrode respectively. The devices were tested in air using a manual probe with a Keithley 4200SCS analyzer at room temperature and elevated temperatures.

3. Discussion

Dual-sweep I_d-V_g curves of the SWCNT-TFT are shown in Fig. 1, where V_d = -1 V and V_s = 0 V. Hysteresis of > 220 V is obtained, indicating a large amount of negative charge is generated (~2.6 x 10^{-6} C/cm^2). To reveal the origin of the hysteresis, comparative TFT with the same structure, fabricated by using SDS sorted SWCNTs has been measured. The hysteresis is confirmed to be much smaller than that of the PCz sorted SWCNT-TFT, which strongly suggests the surrounding PCz polymer may be the main source of the hysteresis. Fig. 2 shows the I_d-V_g characteristics with various V_d, asymmetry forward and backward curves are observed. The backward curves (on the right) show obviously steep slope than the forward ones, indicating the coexistence of some other mechanism that modulates the channel carrier concentration. Fig. 3 shows the I_d-V_g curves with very slow sweep rate by changing the step, which were measured immediately after applying V_g = -50 V for 2 s. Notably, the steep SS breaks the Boltzmann limit, and reaches <10 mV/dec for 0.2 mV step case. The electric field modulation during this test is negligible because the V_g range is very narrow and close to zero. Therefore, we think a certain PCz related electrochemical reaction is the main cause of the steep slope. To understand the reaction kinetics, we measure the I_d-time curves after V_g stressing under various measurement temperature, as shown in Fig. 4. Under the assumption of the following reaction, $[PCz]^-$+h= [PCz]= $[PCz]^+$+e, the activation energy of the reactions and free energy diagram can be calculated based on the I_d-time characteristics with elevated temperature, as shown in Fig. 5. Assume the initial charge in PCz is neutral in the equilibrium state, after applying negative gate bias, the PCz is positively charged and thus results in the depletion of SWCNT channel. When release the negative gate bias, the surface charge recovery is driven by thermal reaction, in which charge transfer by absorbing the electrons in the air may occur, with a barrier of 0.20 eV. Similarly, when the surface is negatively charged, recovery from accumulation to equilibrium contains a barrier of 0.08 eV. Fig. 6 demonstrates an electronic timer application based on the 8000 s I_d-time characteristic for the hysteric SWCNT-TFT. After an initialization with strong negative bias, no matter there is current goes through the channel or not, time dependent modulation of the channel carrier concentration always occurs. Under the energy stored in the hysteresis, such type of device can be used, e.g. to count the time, even under power-off state.

4. Conclusions

Hysteric PCz sorted SWCNT-TFTs with very steep SS (<10 mV/dec) have been demonstrated. Electrical field induced charging and thermal driven discharging of the surrounding PCz polymer are revealed to be the main reason of the hysteresis and the steep slope. Activation energies of 0.20 eV/0.8 eV are extracted for positively/negatively charged PCz polymer to recovery. Finally, for the first time, an ultralow static power consumption timer application is demonstrated, opening a great potential for future ultralow power application.

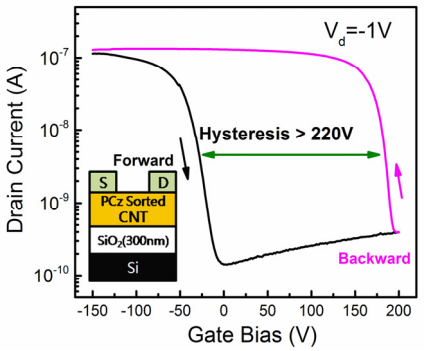

Fig. 1 The I_d - V_g curves of a fresh sample with channel size of 50 μm/ 100 μm (L/W) under drain bias V_d = -1 V and source bias V_s = 0 V. Hysteresis of over 220 V is demonstrated. Sweeping rate of the gate bias is 3V/s with step of 0.5 V.

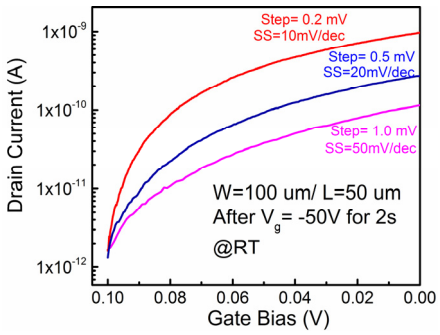

Fig. 3 I_d - V_g curves with very slow sweep rate by changing the step, which were measured immediately after applying V_g = -50 V for 2 s. Notably, the steep SS breaks the Boltzmann limit, and reaches <10 mV/dec for 0.2 mV step case.

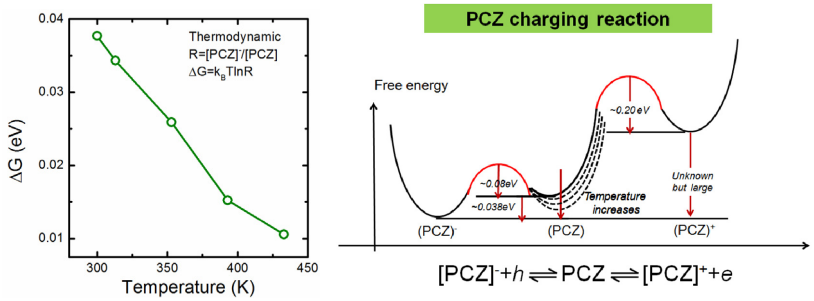

Fig. 5 The free energy diagram and activation energy of the surface electrochemical reactions [PCz]$^-$+ h= [PCz] = [PCz]$^+$+ e, which are calculated based on the I_d-time characteristics with elevated temperature.

Acknowledgements

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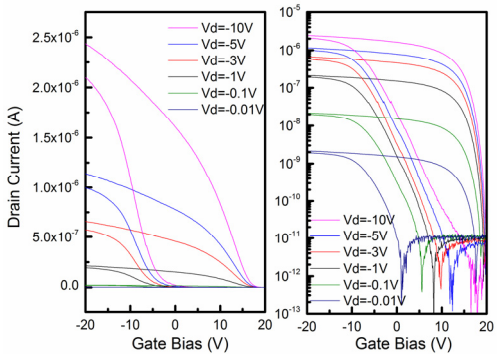

Fig. 2 I_d-V_g characteristics with various Vd, asymmetry forward and backward curves are observed. The backward curves (on the right) show obviously steep slope than the forward curve.

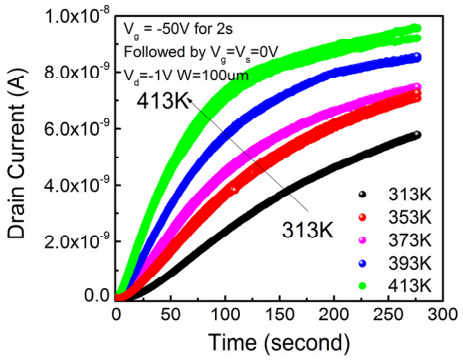

Fig. 4 I_d-time curves after V_g stressing under various measurement temperature of 313, 353, 373, 393 and 413 K.

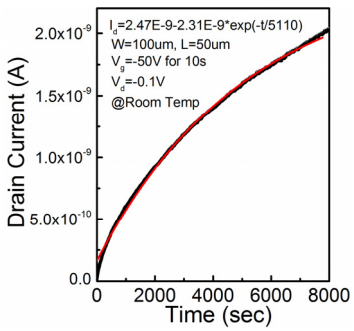

Fig. 6 Demonstration of an electronic timer application based on the 8000 s I_d-time characteristic for the hysteric SWCNT-TFT.