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Strong *p*-type SnS FETs: From Bulk to Monolayer

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Abstract

Characteristics of SnS FETs are systematically investigated with changing the number of layers. An intrinsic *p*-type conductivity and heavy doping at the order of 10^{19} cm^{-3} are observed. Although, for SnS thicker than 9 layers, the gate tuning behavior is weak due to a finite max. depletion width of W_D~5 nm, fully depleted behavior is achieved for 5-layer-thick SnS at RT.

1. Introduction

Two-dimensional (2D) SnS, whose crystal structure is viewed as rows of two orthogonally coupled hinges similar to black phosphorus (BP), has been recently attracted attention for its strong anisotropy and *p*-type conductivity with a high theoretical carrier mobility over 10,000 $cm^2V^{-1}s^{-1}$ [1]. Compared with MoS_2 with large effective mass due to Mo-*d* orbital, SnS and BP have small effective mass due to S-*p* and P-*p* orbitals, respectively. Furthermore, the deformation potential of SnS is smaller than that of BP, which results in higher mobility along the armchair direction [1]. However, electrical transport characteristics are unexplored for few-to-monolayer SnS [2], because the isolation of monolayer is prevented by a strong interlayer force owing to the lone pair electrons in Sn atoms [3]. In the case of SnSe, field-effect transistors (FETs) have been reported for monolayer prepared by the post-thinning method, whereas quite a weak ambipolar behavior was observed probably due to additional extrinsic *n*-type doping by the extra vacancies [4].

In this work, high quality SnS layers were fabricated from bulk to monolayer via Au-exfoliation [5] and physical vapor deposition (PVD). We demonstrate few-to-monolayer SnS FETs for the first time. The thickness dependence is systematically discussed.

2. Device Fabrication

Bulk-to-monolayer SnS layers were fabricated on 90-nm SiO_2/n^+-Si and mica substrates via the Au-exfoliation and PVD, respectively, as shown in **Fig. 1**. Ni (or Ni/Au) was deposited as source/drain electrodes. **Fig. 2** shows cross-sectional illustrations and optical images of SnS FETs. Back-gated FETs were measured for SiO_2/n^+-Si substrate. For mica substrate, top-gated FETs were fabricated with 15-nm-thick Er_2O_3 insulator (effective ε = 4.5–6.0) and Al top-gate electrode. To prevent the degradation of SnS, Er_2O_3 was deposited at RT via thermal evaporation in the specially designed chamber, where oxygen pressure was controlled for the sample and Er source separately [6]. Electrical transport measurements were performed at different temperatures in the range of 150–300 K.

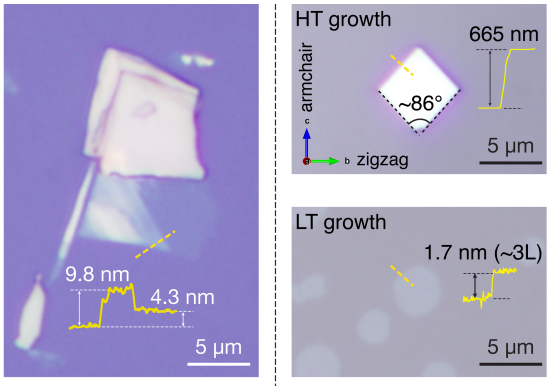

Fig. 1 Typical optical images of SnS via (a) Au-exfoliation and (b) PVD. Insets: AFM height profiles along the dashed lines.

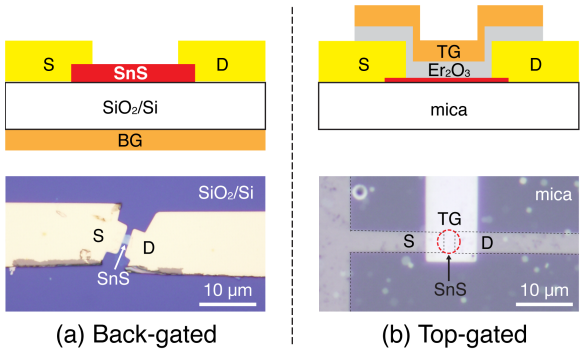

Fig. 2 Cross-sectional illustration and optical image of (a) back-gated and (b) top-gated FET.

3. Results and Discussion

After the Au-exfoliation, ultra-thin flakes were obtained with large size owing to the strong semi-covalent bonds between Au and S atoms [5], as shown in **Fig. 1(a)**. The flake thickness was distributed from several hundreds of nm to 1.1 nm, which is close to the monolayer thickness. High quality SnS layers were confirmed down to 9 layers (9L) by cross-sectional transmission electron microscopy, whereas optically/electrically active monolayer SnS was not realized due to the oxidation during Au etching in an oxidative KI/I_2 solution [5]. For the PVD grown SnS, crystal thickness was controllable with changing the growth temperature, as shown in **Fig. 1(b)**. Diamond-shaped bulk crystal was ob-

tained at high temperature (HT), while few-to-monolayer crystal with rounded shape was obtained at low temperature (LT). Monolayer-thick (~0.7 nm) crystal via PVD was Raman active unlike that via Au-exfoliation. These results suggest that bottom-up process is superior to top-down one in terms of the crystallinity of monolayer SnS. **Fig. 3(a)** shows the electrical transport characteristics as a function of the back-gate voltage at RT and V_D = 1 V, for different SnS thicknesses: 9L, 12L, and 16L. Although all FET devices showed *p*-type characteristics, the device was not turned off with the back-gate modulation even for 9L. The field-effect mobility μ was estimated using the following equation:

$$\mu = \frac{L}{W}\frac{g_m}{C_{ox}V_d}, \text{ where } g_m = \frac{dI_d}{dV_g},$$

where L and W are the length and width of the channel, and C_{ox} is the gate capacitance. The μ for 9L, 12L, and 16L were determined to be 0.47, 0.18, and 0.05 $cm^2V^{-1}s^{-1}$, which are comparable to the reported μ of 10 nm (~18L) SnS ranging from 0.2 to 1.1 $cm^2V^{-1}s^{-1}$ [2]. **Fig. 3(b)** shows the temperature dependence of transfer characteristics. The off-state appeared only when the temperature was decreased, which is in contrast to that of typical 2D channels, such as MoS_2. This is because the carrier concentration is significantly reduced by the freeze-out of holes from acceptors.

Fig. 4(a) shows the electrical transport characteristics of PVD grown 5L SnS as a function of the top-gate voltage at RT and V_D = 1 V. In contrast to the thick SnS (>9L), 5L SnS exhibited the off-state at RT. Herein, for the first time, the intrinsic *p*-type and fully depleted FETs was demonstrated for few-to-monolayer SnS.

Fig. 5(a) summarizes the SnS thickness dependence of current modulation I_{ON}/I_{OFF} from this work and the reported

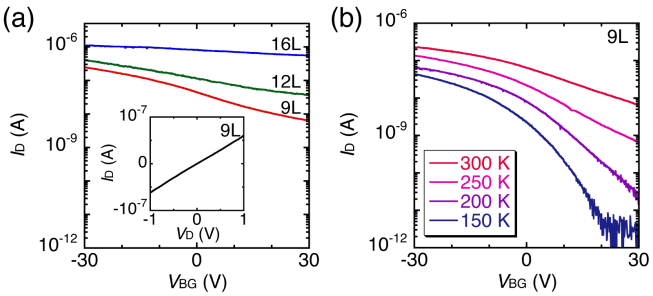

Fig. 3 (a) I_D–V_{BG} plots with the different number of layers at RT and V_D = 1 V. (b) I_D–V_{BG} plots of 9L in 300–150 K at V_D = 1 V.

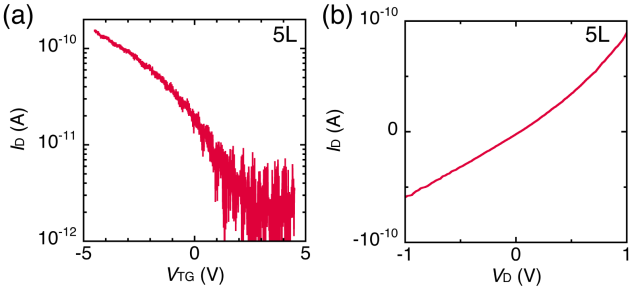

Fig. 4 (a) I_D–V_{TG} plot at V_D = 1 V and (b) I_D–V_D plot at V_{TG} = 0 V of 5L SnS at RT.

thinnest SnS FET [2]. The transition occurs at ~5 nm, which is much smaller than MoS_2 FETs (48–55 nm [7]), suggesting the heavy doping in SnS to limit the depletion width W_D. To estimate the acceptor density N_A of SnS, a simple calculation was performed using the maximum depletion width W_D as follows:

$$W_D \approx \sqrt{\frac{2\varepsilon k_B T \ln\left(\frac{N_A}{p_i}\right)}{e^2 N_A}},$$

where p_i is the intrinsic carrier concentration, and ε is the dielectric constant of SnS, roughly estimated using the relative dielectric constant of ~10. The p_i of thin SnS is estimated using the equation $p_i = 10^{18}\exp(-E_g/2k_BT)$ with the bandgap E_g = 1.1 eV. In **Fig. 5(b)**, the relationship between W_D and N_A of SnS at RT is shown. By equating W_D to these SnS thicknesses, N_A is estimated to be of the order of 10^{19} cm^{-3}, which is consistent with the previous estimation [8]. Although I_{ON}/I_{OFF} = ~10^2 of 5L was much higher than thicker ones, further performance can be expected since the high-crystallinity for as-grown crystals has been confirmed by Raman measurement. Improvement of device fabrication process enables to extract original features of few-to-monolayer SnS.

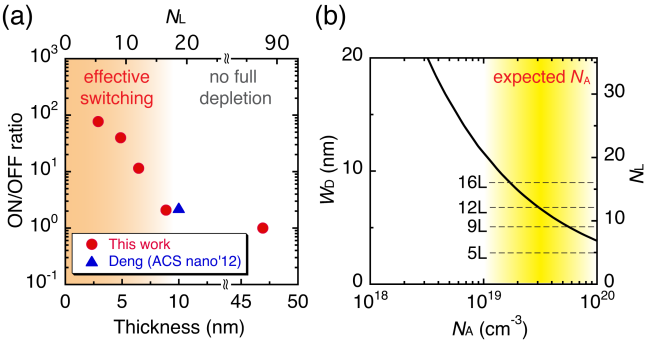

Fig. 5 (a) Current modulation I_{ON}/I_{OFF} versus thickness. (b) Relationship between depletion width W_D and acceptor density N_A.

4. Conclusions

The characteristics of SnS FETs were systematically investigated with changing the number of layers. The intrinsic *p*-type conductivity and heavy doping at the order of 10^{19} cm^{-3} were observed. Although, for the SnS thicker than 9L, the gate tuning behavior was weak due to the finite max. depletion width of W_D~5 nm, fully depleted behavior is achieved for 5-layer-thick SnS at RT.

Acknowledgements

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