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Novel InAs/GaSb Heterostructure Nanowire Based Tunnel Field Effect Transistor

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Abstract

We study the growth of high crystal quality external catalyst free InAs/GaSb heterostructure nanowires on Si (111) substrate by metal-organic chemical vapor deposition (MOCVD). GaSb was grown axio-radially on InAs nanowires. GaSb shell thickness was controlled by growth time. With good quality NWs and control on GaSb shell thickness, the effects of device intrinsic parameters such as shell thickness, spacer length are investigated on the performance of InAs/GaSb nanowire Tunnel Field Effect Transistors using TCAD simulation. Device on-current (ION) was chosen as the key figure of merit. Found that ION can be improves by adding spacer upto a critical limit.

1. Introduction

The InAs/GaSb heterostructure NWs has been investigated for various device applications due to it's exotic type II broken band alignment and free standing nature which can efficiently relax the lateral strain [1]. Steep-slope devices, such as TFETs, have recently gained a lot of attention due to their potential for low power operation. TFETs are based on band to band tunnelling (BTBT) which could limit the on-current since the charge carriers must tunnel through a barrier. This InAs/GaSb type II broken gap band alignment is considered as an ideal system for devices like TFET.

2. Nanowire Growth

All nanowires used in this study were grown using MOCVD. Growth and control over morphology of gold-free InAs and InAs/GaSb heterostructure NWs by growth temperature have been studied and reported previously [2]. In this study, a very good crystal quality InAs and InAs/GaSb heterostructure NWs were grown using optimized growth conditions and GaSb shell thickness was controlled by varying growth time. All the NWs were characterized by Field-emission Scanning Electron Microscope (FE-SEM), High Resolution Transmission Electron Microscope (HRTEM) and X-ray Energy Dispersive Spectroscopy.

3. Device Structure and Simulation

In this work, a core-shell nanowire structure of InAs-GaSb and 50nm drain and channel length is considered (Fig. 1). Doping of InAs core, for drain is taken as 2e17 and for GaSb shell is taken as 4e19. Extensive device Simulations were carried out using Synopsys's Sentaurus TCAD. Lombardi mobility model, Band-gap narrowing was included in the simulations. Dynamic non-local BTBT was also included in the simulations. WKB approximation was used in order to calculate the tunneling rate in the simulations.

4. Results and Discussion

A. Growth of InAs / GaSb Heterostructure Nanowire

Figure 1 shows InAs NWs grown at 600 °C with a fixed growth time (150 sec) and fixed TMIn (2.9×10^{-5} moles/min) and AsH3 (4.5×10^{-3} moles/min) flow rates. These optimized growth parameters resulted in a good crystalline quality wurtzite (WZ) (Fig 2) InAs NWs. Using this as the core, GaSb were grown with varying growth time between 4 min to 14 min at fixed growth temperature of 530 °C and V/III ratio of 1.0. Figure 3 shows InAs/GaSb heterostucture NWs. WZ crystal structure of the InAs core was transferred successfully to GaSb shell through layer by layer radial growth (Figure 3). Figure 4 shows InAs/ GaSb NWs grown with various GaSb growth time. As the time increases from 4 min to 14 min, GaSb shell thickness linearly increases from 12 nm to 42 nm.

B. Simulation study on effect of Shell Thickness

Impact of GaSb-shell thickness on the device performance is examined at 300K in Fig. 5. When the shell thickness is less, the resistance across the device is less, this results in higher on-current. From the band diagram (Fig. 6), it is evident that due to larger band bending for 18nm shell radius, device on-current is higher. For shell with radius of 18nm, e-density is more in the channel as compared to 25nm, thus the charge carrier in the channel is more, hence increase in on-current.

C. Simulation study on effect of spacer length

To further improve the device performance, a 2nm thick Si3N4 spacer was added at the source-channel junction. Low-k spacer at the junction results in better gate coupling which results in the reduction of device threshold. As the gate voltage is increased, source starts to deplete due to the fringing field induced by the gate. Due to the gate fringing field through the high-k spacer, electric field shifts more towards the source. This results in decrease in tunneling barrier width which in turn results in higher on-current (Fig 7). As the spacer length increases beyond a critical limit, on-current starts to reduce. This is due to the increase in tunneling barrier width between source and channel.

5. Conclusions

A growth of high crystal quality InAs/GaSb heterostructure nanowires by MOCVD is demonstrated. GaSb shell thickness was controlled by using growth time. Using TCAD simulation, the effects of shell thickness and spacer length on the performance of InAs/GaSb nanowire TFET is investigated. Device on-current (ION) was chosen as key figure of merit. It is found that ION can be improved by adding spacer upto a critical length.

References

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[2] R.K.Kakkerla, D.Anandan, C.J.Hsiao, H.W.Yu, S.K.Singh and E.Y.Chang, J.Cry.Growth, 490 (2018) 19.

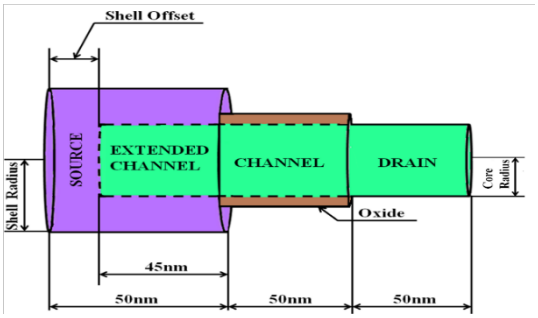

Fig 1 GaSb/InAs core-shell nanowire TFET structure

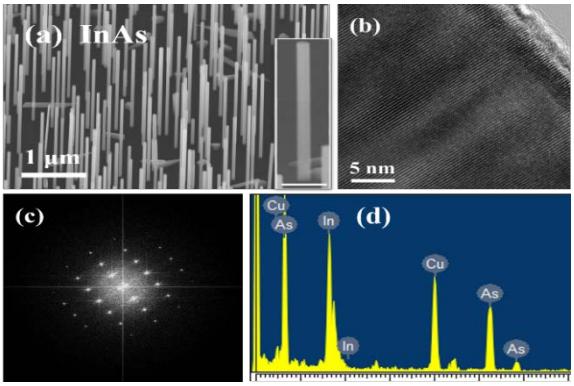

Fig 2 InAs NWs (a) 45° tilted view SEM image (Insert is high magnification image with scale bar 200nm) (b) HR-TEM image(c) Corresponding FFT (d) EDX profile

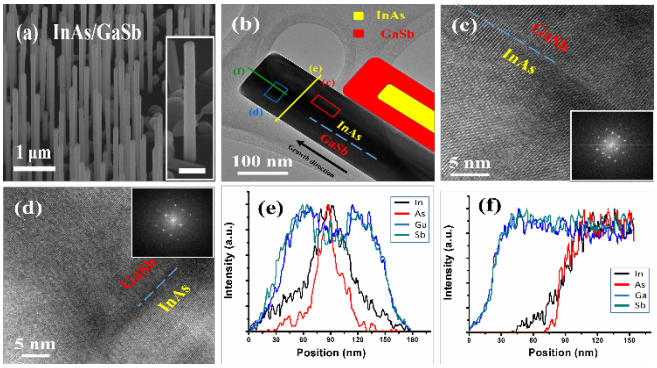

Figure 3 InAs/GaSb NWs (a) 45° tilted view SEM image (Insert is high magnification image with scale bar 300nm), (b) Low magnification TEM image, (c) HR-TEM image along radial direction (Insert corresponding FFT), (d) HR-TEM image along axial direction (Insert corresponding FFT) (e) EDX profile along radial direction, (f) EDX profile along axial direction

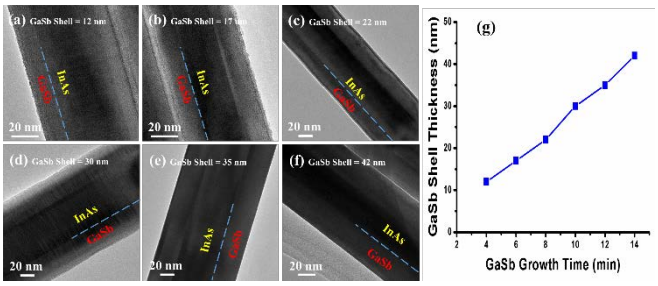

Figure 4 InAs/GaSb NWs with different GaSb shell thickness (a) 12 nm (4 min), (b) 17 nm (6 min), (c) 22 nm (8 min), (d) 30 nm (10 min), (e) 35 nm (12 min), (f) 42 nm (14 min), (g) graph between GaSb shell thickness Vs growth time.

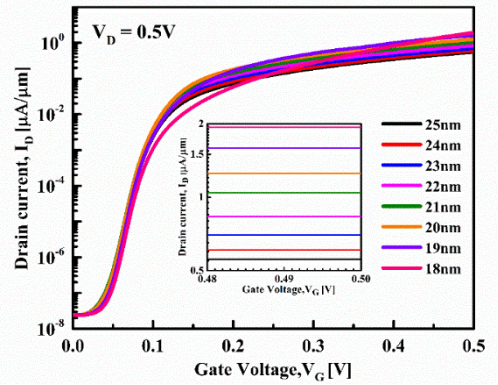

Fig 5 Id-Vg characteristics of different shell thickness of Core-Shell nanowire TFET varying from 18nm-25nm

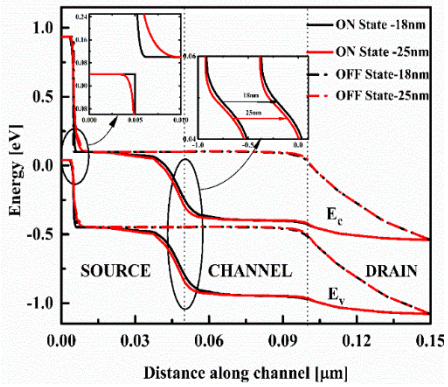

Fig 6 Band diagram of core-shell nanowire TFET with 18nm and 25nm shell radius

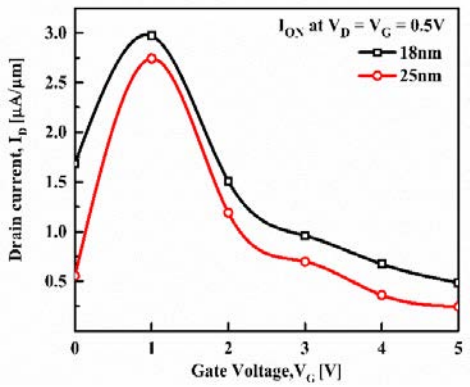

Fig 7 Ion vs spacer distance for 18nm and 25nm core-shell nanowire